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*Research Paper*

# The proposed model of pulse code modulation encoder for voice frequencies

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## Abstract

In this paper, we have developed a hardware-based model of pulse code modulation (PCM) system for voice frequencies. Firstly, we have constructed sample and hold circuit using triggered semiconductor switch (e.g., MOSFET), which is capable of sampling voice signals at 8 kHz according to Nyquist theory. Then an Analogue to Digital Converter (ADC) Integrated Circuit (IC) is introduced to quantize and to digitize of the output of the sample and hold as pulse amplitude modulation (PAM). The converted outputs are 8-bit digital parallel value per sample at a frequency of 8 kHz. Finally, a parallel to serial converter logic is constructed which remains the voice frequency at the accurate time without any delay. The principle feature of this PCM system is that during a final interval of time, it makes a waveform into 8 bit serial code word. An 8-bit shift register with decade counter and flip-flop based logic are providing to this wave-from one after another without any interruptions of the sequences.

***Keywords***: *Pulse Code Modulation (PCM); Nyquist Theory; Sample and Hold; Analogue to Digital Converter (ADC); Shift Register; Decade Counter; and Flip-Flop.*

## 1. Introduction

A speech signal is a sound which is the way of communication with human. It travels in the form of a sound wave using atmospheric pressure and widens in the air [1]. If we want to transmit voice signal over any communication networks, then the voice signal has to be converted from sound wave to an electrical signal. A microphone performs this conversion. The result of a microphone is an electrical signal where the voltage varies with the pressure of the speech signal [2]. The output of the microphone (electrical signal) is also known as analogue signals. Earlier communication systems were used to transmit and to receive in the form of electrical analogue speech signals from one place to another. In the primary era of communication development, human established some analogue communications system. But a number of shortcomings were observed using analogue communication. For example, when analog signals become weak because of transmission loss, it is hard to separate the complex analog structure from the structure of random transmission noise. In the receiver, the device needs to amplify analogue signals to return back the original speech, it also amplifies noise, and ultimately analogue communications system becomes too noisy to use [3].
In the modern era, digital communication system has been invented to overcome limitation of analogue communications system. Digital signals are easier to separate from noise and can be constructed return into original shape. The conversion of analogue signals to digital signals is the primary process of digital communication system which eliminates the problems caused by attenuation. Pulse Code Modulation (PCM) is the simplest form of waveform coding amongst other conversion processes as like Adaptive Pulse Code Modulation (APCM), Delta Modulation, etc. Waveform coding is a process to encode analogue signals (for example human voice) into digital code word. The digital signal is subsequently reconstructed back to the analogue signal at the receiver [4]. Digital communication system is the transformation of data over a point to point or point-to-multipoint communication channel using any proper

communication medium such as copper wires, optical fibers, and wireless. The data is represented in any form of signal such as electromagnetic signal, electrical voltage, radio waves, optical signal or microwaves [5].
Modern telecommunication system in duplex mode, people could be able to communicate both ways at a time. Each side of a telephone system must be able to code and decode of voice data and vice versa. The process of coding and decoding of the speech signal is performed using speech compression algorithms. Waveform-based speech compression algorithms are the simplest form of speech compression algorithms. The compressing algorithms represent individual samples from the analogue voice waveform into a digital code word. There are three possible ways can be implemented of speech compression algorithms such as software, hardware-software co-design, and hardware [6]. We have implemented the PCM encoder by using hardware only. To design the PCM in hardware, we have maintained every step of the PCM theory in a sequence. We have also maintained ITU-T recommended G.711 standard.

## 2. Literature review

A PCM system is a digital representation of an analogue signal where the magnitude of the analogue signal is sampled regularly at uniform intervals, with each sample being quantized to the nearest value within a range of define digital steps [8]. The PCM is also a waveform coding method defined in the ITU-T G.711 specification [7]. The major parts of a telephone conversion system are the encoder (the analogue-to-digital converter) and the decoder (the digital-to-analogue converter). Encoder and decoder are defined as codec in combine. A PCM encoder performs mainly three functions; sampling, quantizing, encoding [6]. Some steps are followed to convert the analogue voice signal into a digital pulse train. First step is to filter out the higher frequency components of the signal to prevent aliasing. A band-limiting filter is used which has a bandwidth of 4000 hertz. The second step is to sample the filtered input signal at a constant sampling frequency. The original analogue signal can be reconstructed the sampling frequency is at least twice the highest frequency of the original input analogue voice signal is also called Nyquist rate. The original signal can be reconstructed back by a low-pass filter at the destination. The Nyquist criterion is stated like this:
$Fs > 2(BW)$
Fs = Sampling frequency
BW = Bandwidth of original analogue voice signal
After filtering and sampling the input analogue voice signals, the next step is to digitize each sample. The PCM system has an analogue-to-digital converter. The quantization is a technique to encode the Pulse Amplitude Modulation (PAM) samples. The process of converting each PAM sample's value into a discrete value which is assigned a unique digital code word is called quantization. When the input PAM samples are entered into the quantization phase, all samples are assigned to an individual quantization interval. In the uniform quantization, all intervals are equally spaced over the range of the input analogue signal. Each quantization interval is assigned a discrete value in the form of a binary code word. The output of ADC has a standard word size equal to eight bits. As the analogue signal is sampled at 8 kHz with 8-bit code word, so the maximum transmission rate will be 64k bits per second for voice signal.
If an input PAM sample is not matched (matches its actual height) with assigned a quantization interval, then an error is generated in the PCM process. This error is called quantization noise. To get a better voice quality in any communication system, the SNR should be higher. Quantization noise caused by mismatch sample with assigned high reduces the SNR of a signal. As a result, degrades the quality of a voice signal happened. The solution of quantization noise is to increase the amount of quantization intervals. With the increase of quantization interval, more code word is generated; also bandwidth increased which introduce an additional problem to deal with PCM system. We can also avoid this problem by increasing the quantization level into higher signal levels as most voice signals generated at low frequency. This is a very inefficient way of digitizing voice signals to improve voice qualities which replace uniform quantization defined as non-uniform quantization. This is also called companding. The term companding is a combination of the two terms, compressing and expanding. During the companding process, input analogue signal samples are compressed into logarithmic manner. After compression, each segment is quantized and coded using uniform quantization. The larger sample signals are compressed more than the smaller sample signals [5].
There are several types ADC to convert the signal into digital form. Among those, we have used successive approximation ADC in our circuit. A success approximation is a ramp type of ADC, which specially designs to reduce conversion and to increase operational speed. In this type, a counter is used to resent after every sampling interval to generate digital outputs. The counter starts the process of counting for 0 and it adds to LSB, clock pulse goes up to 2N to reach maximum value [16].
Some of the similar systems are already established in the form of software, hardware or both. Researchers implemented hardware of the pulse code modulation encoder and decoder (PCM Codec) that aims at improving the delay of the speech compression of this codec specially to improve Quality-of-Service (QoS) of VoIP Telephony [9]. Tomar and George implemented PCM in hardware that was able to significantly reduce algorithmic delay (latency) of the Pulse Code Modulation (PCM) speech compression algorithm. Earlier, it was implemented in software [7]. Whalen, Wiley, Rubin, and Cooper of Haskins Laboratories have encountered some solution of earlier problems of PCM system [10]. They have installed the Nyquist filter response; the high frequency pre-emphasis filter characteristics; the dynamic range; the timing resolution, for single and dual channel signals; and the form of the digitized speech files along with

other laboratory system [10], [11]. Cattermole described the impact of pulse code modulation on the telecommunication network. He considered junction transmission, trunk transmission, tandem switching, group selection in terminal exchanges and integration over limited areas in his paper [12].

# 3. The model of PCM system design

According to PCM theory, we have demonstrated the following system to implement in real voice signal of single band signal 300-4000 Hz. We have incorporated a filter to remove unwanted single and to prevent aliasing just before the start to converting the signal from analogue to digital. We have followed through a simple process of PCM theory: firstly, the output of filtered electrical signals for voice are sent to sample and hold circuit for sampling and initial task of quantization functions; secondly, we have added an ADC IC which is capable to convert reference input DC voltage levels into 8-bit digital information in the middle of the circuit. The final function of our circuit is the conversion of all parallel out bits into serial form to transmit through a standard digital communications channel.

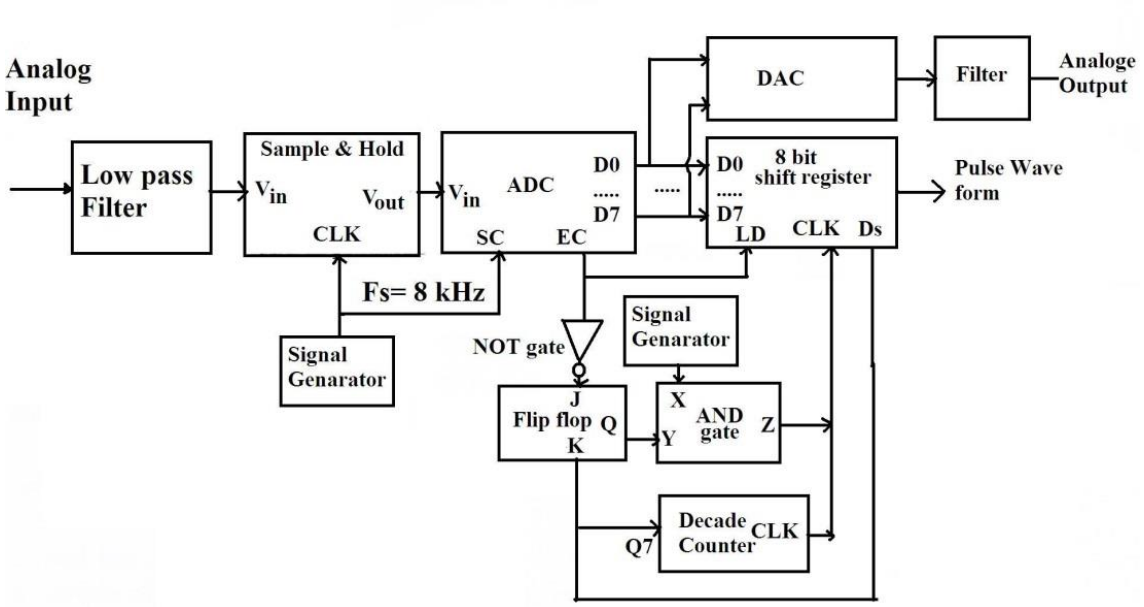


**Fig. 1:** Block Diagram of the Model of PCM System

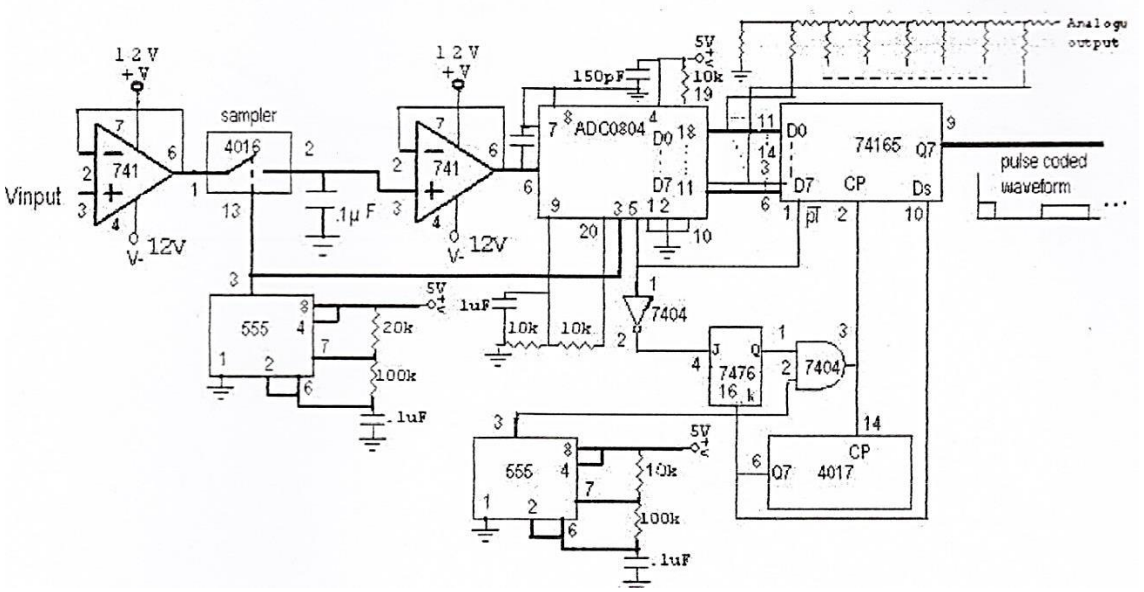


**Fig. 2:** PCM System Connection Diagram.

The following connection diagram (fig. 2) contains a full implementation of the PCM system that we have designed. Initially, a conventional low pass filter is introduced for preventing the alias of voice signals. The sampling function is done by combining two operational amplifiers (741) and a MOSFET (4016). The buffer function is for buffering the signal for a while, and then buffer signal goes for the switching function for sampling the input applied signal at rate of

8 kHz. A hold capacitor is used to hold sampled signals. Then, the output of the sample and hold circuit is sent to IC ADC 0804 for digital conversion. The IC ADC requires resistors and capacitors that are connected to different specified pins. The IC ADC is capable to convert each reference voltage as defined into 8-bit digital form in parallel out for each sample. The final task is to convert the whole parallel output in serial form, but keeping the sequence and time of the individual quanlized sample, done using specially design logical circuit.
We will describe this project through the following different steps:

- Sample and hold operation.
- Quantized and digitized each voltage level with parallel output.
- Parallel to serial conversion.

## 3.1. Sample and hold operation

Filtered analogue voice signals are applied to convert at digital form into the sample and hold circuit. It takes sample at a rate of constant sampling frequency 8 kHz. we has designed such a sample and hold circuit which is designed by combination of two operational amplifiers and a MOSFET switch as an analogue voice frequency sampler. We have applied a pulse train of constant amplitude and frequency that is generated from a timing generator (IC 555). Input voice signal accomplished with pulse train and generated a pulse amplitude modulation (PAM) signal.

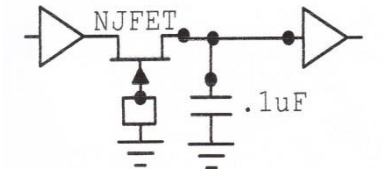


**Fig. 3:** Sample and Hold Circuit

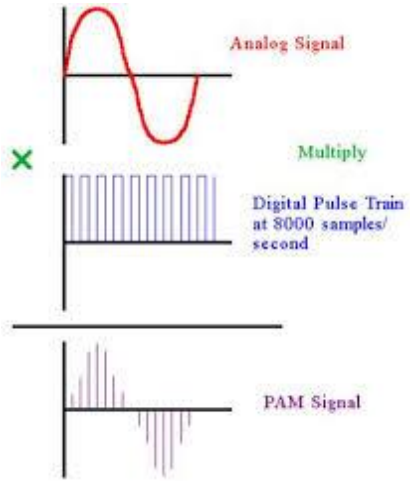


**Fig. 4:** Steps Shows to Convert Analogue Signals into the PAM Signal.

The circuit (fig. 3) contains a pair of buffer amplifier, sampler, pulse generator and hold capacitor. The activities of the sample and hold signal has shown in fig. 4. The operation of the buffer amplifier is to remain input to the output, but the benefit is the input resistance infinity and the output resistance is zero, as a result the operation of hold time constant is zero. This is used for not to affect the input signal, i.e. baseband signal as input resistance is infinity. It provides a gain of unity without any phase reversal. The 4016 MOSFET switch takes a sample of analogue signal and after 80 µSec, it takes another sample and so on. The capacitor is charged while a sample value found. The pulse generator is made using 555 timers IC. It will provide pulse 8000 per second, which is needed for sampling analogue signal and to start conversion. This sampling rate is designed in accordance to sampling theorem. When the capacitor is discharged, then input sampler is off, so the signal goes through the output buffer and in this way sample and hold signal is generated. The output signal of our designed sampler is called discrete signal, but still continuous valued. So the signal is required to change into the hold to constant levels of each sample that is called sample and hold signal. The hold activity is performed by a capacitor as the input resistance of the capacitor is zero so that no time delay will be occurs.

### 3.1.1. The pulse generator

The pulse generator (fig.5) contains an IC 555, two resistors, and a capacitor. The capacitor and resistors control the pulse width (active high and active low), frequency, and time and duty cycle. We can generate any shape of rectangular wave by changing the value of the resistor.

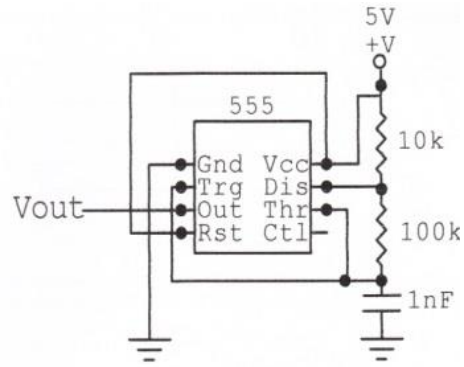


**Fig. 4:** The Pulse Generator for Controlling the Sample Signal Data Rate.

Time duration and frequency of pulses:
Ton=0.693(R1 + R2) C; Toff = 0.693R2C; T = 0.693(R1 + 2R2) C

$$f = \frac{1.44}{(R1 + 2R2)C}$$

Duty cycle:

$$d = \frac{Tm}{Ton+Toff} = \frac{R1+R2}{R1+2R2}$$

We have designed two timing generators by using the previous formula of T and f for the following two purposes:

- Sampling and start conversion having a frequency, fs=8 kHz.
- To convert data from parallel to serial, we need 80 kHz frequency for each sample.

The duty cycle should not be larger than 40% of T. We have applied 10% of the duly cycle in our proposed model.

## 3.2. Quantized and encoding

The basic task of A/D converter is converting a continuous range of input amplitudes into a discrete set of digital code words. This conversion involves the processes of quantization and coding. We have used such an ADC IC which is capable to convert un-uniform quantization levels. ADC 0804 is a successive approximation converter. The sample and hold signal (fig.3) applied to ADC, but assigned quantization intervals of the ADC are equal. Beyond assigning quantization interval, ADC considers other level according to the approximation of amplitude, and high of the sample and hold signals. Sometimes discrete amplitude holds the signals' high, that are not matched with level defined, then equalization errors occur. For example, if the ADC responses quantization level at 95 mV, the ADC will consider the sample value at 90 mV. This is the process of comparing approximation quantization of non- marginal input into digital. All quantization levels (fig.6) are specified according to the voltage level in sequence. Each quantized level is addressed unique 8-bit code word. The ADC 0804 IC is defined voltages starting from 0 to 127 in positive and negative side. So the quantization levels of the ADC 0804 are 256 numbers in total.
Our input voice frequency is up to 4 kHz. This signal is sampled at 8000 times per second. The ADC 0804 converts each sample at 8-bit standard code word. As a result, the maximum bit rate will be 64000 bits per second

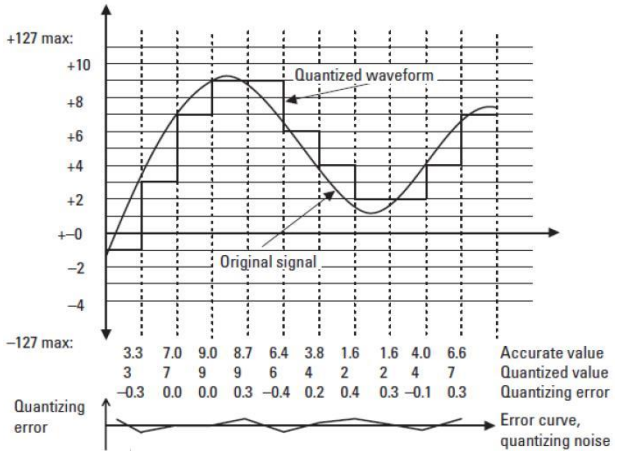


**Fig. 6:** Quantized Level Consideration of Uniform Quantization and Its Error.

The first level of quantization starts from 0 mV then 20 mV and so on. So, the step size between quantization levels has been set at 20 mV. Each voltage has its representation of a binary form starting from 0000 0000 for zero up to 1111 1111 for -127. ADC 0804 is capable to consider the theory of linear quantization. ADC 0804 refers an equal quantization level of all input voice signal. The choice of voltage levels is guided by two constrains. Firstly, the quantized intervals between the levels should be equal; and secondly, it is convenient for the levels to be symmetrical about zero. Each sample is assigned to 256 levels or 8-bit PCM sequence. We used some sub-circuit in different pin with ADC 0804 for different purposes. These sub-circuits are described as followings:

### 3.2.1. The sawtooth wave

A sawtooth wave is required for the ADC doing internal functionality. A sawtooth wave generator (fig.7) is prepared using a resistor and a capacitor to control the conversion time of ADC 0804. We have connected sawtooth wave generator at IC ADC using one resistance (10kΩ) in between pin no 19 and 4, moreover a capacitor (150pF) at pin no 4 to the ground.

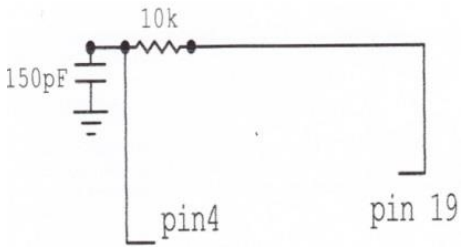


**Fig. 7:** Shows Circuit Diagram for Generating a Sawtooth Wave to ADC.

The time require for the sawtooth wave is calculated by the equation of time constant, T=RTCT . If we submit the resistor and the capacitor value at the previous equation, the resultant time of the sawtooth wave became, T=1.5 µSec.

### 3.2.2. Low clock to indicate end of conversion

The internal arrangement of the ADC is required to indicate a signal low at interrupt pin 5, just after conversion processes are performed. It says that data is now available at the output line for only 100 µsec. When one pulse of 100 µsec is over, then another low pulse (fig. 8b) will be generated with the same duration.

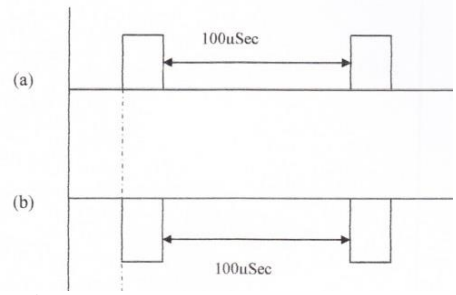


**Fig. 8:** (A) Shows Conversion Time of IC, (B) the Generating Pulse Into Ics Pin 5 (in Fig. 3.5 Connected A Led To Test).

i) Potential divider and resolution output

The ADC is required to operate at a voltage level of 5 V DC. We have supplied an input voltage 5V into pin 20. But another power source of half of the input voltage is required for the system to supply at pin 9 of ADC 0804. A potential divider (fig.9) technique has helped to do the task. We have connected a wire to pin 9 of ADC in between the center point of two-resistor (20 k each). A resistor will be connected to the original source voltage (Vcc, 5 V DC) and other will goes to ground.

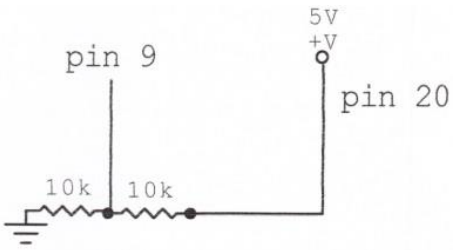


**Fig. 9:** Potential Divider with 2.5 V Output Quantization Characteristics of This ADC Converter.

Now, we will calculate the voltage of the quantizing interval of the ADC 0804 in this circuit. We have supplied a reference voltage of Vref, 2.5 V from the potential divider to get a resolution output voltage which is quantization interval. The calculation of the resolution output voltage is found by $= \frac{2V_{ref}}{2^N}$ ; Where, N is the number of bit and Vref is the reference voltage. So the quantization interval is:

$R = \frac{2V_{ref}}{2^N} = 19.5 \approx 20$ mV

We found a result of 20mV that clearly shows that the ADC 0304 is able to convert digital from analogue hold single one binary sequence to another at 20 mV gap. In a real time communication system, any delay does not allow during transmission. Hence, the transmission time for each sample must be same, regardless of how many bits represent each sample. When there is more bit per sample is generated by PCM system, bits must move faster to the next stage. The data bit is thus increased, and the cost is greater transmission bandwidth. We have represented PCM digits in the PCM wave form. Finally, we have converted all bits into serial output sequences.

## 3.3. Parallel to serial conversion

Serial conversation is very necessary to transmit whole data over a transmitted network. The output of each code word consists of eight bits per sample, those codes are in parallel. We need to establish a one to one correspondence between code word to transmit over any communication channel. For this reason, we have added a logic circuit to create parallel to serial conversion. Any of several line code word can be used for electrical representation of a binary data stream. By using shift register controlled by a pulse generator and decade counter, we have made the parallel input to line coded pulse train outputs.

While digital output is available on the line, the ADC 0804 generates an interrupt signal having low at pin 5. This low signal will help to load into buffer memory of registers. All registers have shifted every bit from a flip-flop to another, and then goes out. This arrangement is provided from a timing generator (frequency, 80 kHz) and a flip-flop give a bit during set stats. We have used an AND gate to integrate both flip-flop and clock pulse. The input of the flip-flop is an inversion of interrupt signal. We have added a NOT gate to invert at the pin 5 to flip-flop. The activity of the decade counter is counting 8-bit one after another. The counter starts counting and provides a reset to the flip-flop. The output the flip-flop and the counter goes to the parallel to serial converter (fig. 10) at the Ds pin. This function will be continued till second steps of quantized digital output (fig.11).

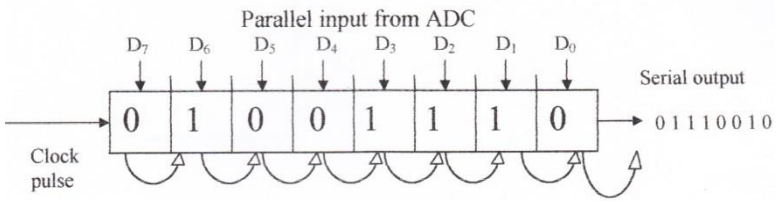


**Fig. 10:** An Example How to Shift 8-Bit of Data.

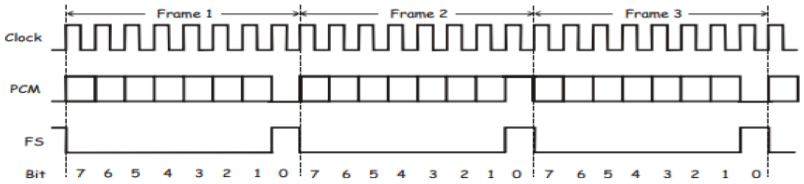


**Fig. 11:** PCM Bit Representation after Parallel to Serial Conversion Process.

The ADC 0804 generates an interrupt signal which is actually a low signal to indicate end of conversion. We have used this signal to load data to shift register and controlling clock pulse. The interrupt signal of the ADC at pin 6 is inverted by using a logical inverter. The inverter is added in between ADC pin 6 and the flip-flop to generate clock pulses to provide a sequential output pulse train. The flip-flop is necessary to store a bit while set stage. It keeps data to send after a sequence and to remain discipline all data one sequence after another. The shift register shifts a bit, it is stored. Then, the flip-flop goes to reset the stage and send another group of code word and so on.

A decade counter (binary counter) with flip-flop is sent output clock pulse in serial to the parallel to serial converter. The function of flip-flop is to hold LSB, then count until the next incoming pulse. The counter count one bit and provide a clock pulse to parallel to serial converter and helps to shift a bit to go the next stage. We need a logical AND here with a decade counter to the synchronies output of JK flip-flop and 555 timer. The timer generated a pulse train at the same frequency that should be similar to the digital output of the ADC. When we will find a pulse from latch (JK) the logical AND will give an output with the pulse of the 555 timer. The combination of two pulses provides pulse at

the "ON" of two pulses of the input of logical AND, gives an output followed through the clock pulse of PISO converter. We have added a timer as a frequency generator up to 80 kHz to control decade counter and shift register at a time as the output of ADC data is same.

# 4. Advantages of hardware implementation PCM encoder over others

The PCM encoder converts data into 8 bits serial pulse train which consists of three basic units. The units are: Sample and hold, Quantization and Encoding and Serial to parallel converter. The input of voice signals has converted by conversion unit with 8 bit uniform format.

We have found lots of superiority among the types of PCM implementation process (Hardware, Hardware and software and only software). Hardware implementation of PCM has been done fully hardware environment using simple electronics components and integrated circuit (IC). We have found expected output without using any complex, expensive programming based PCM system. Our design is simple and easy to understand. Any learner can take helps to learn the basic of PCM system. All results can show individually step by steps such sample and hold, ADC, parallel to serial converter and DAC output. We have designed such a parallel to serial converter which is able to produce serial of the output bit pulse train without effecting synchronization among individual output quantization segments.

Turner and George were done implementation, hardware of the PCM speech compression algorithm in VHDL using the Xilinx 11.1 ISE environment. They used Integer arithmetic and Xilinx IP Core library of the ISE environment. They actually proved to demonstrate that the algorithmic delay (latency) of the Pulse Code Modulation (PCM) in software over hardware [7]. The whole process is expensive and complicated.

Only Software implementation of PCM always may not actual. It requires a computer and software to run this. On the other hand, software based simulation is like dummy activities of PCM for test and study not practical. It also requires a person to implement the sound programming knowledge. This is too much expensive, but not convenient for all environments. This implementation has an algorithmic delay (latency). [7] [9]

There is another type of implementation, hardware and software combination. All functional activities have been written using VHDL language in FPGA number of supportive electronics component are connected. This is fast and more effective using FPGA, but it can be faster using ASIC [7]. Learner on early of study of telecommunication and electronics will face huge difficulties to understand.

# 5. Results

There is nothing physical about the digits, resulting in the general PCM process. Digital are just abstractions a way to describe the massage information. We will represent the binary digits with an electrical pulse according to any standard of code conventions representation such as NRZ-L, NRZ-M etc. Code word time slot is shown where the code word is a 7 bit representation of each quantized sample. Each binary pulse is represented by a pulse and binary zero is represented by the absence of a pulse.

## 5.1. Verification of PCM as a uniform encoder

We have tested (Table 1) our encoder ADC 0804 by applying DC voltages from the power supply. The power sully has the ability to control in mV level. The expected output of our hardware implemented PCM has found according to standard [ITU (1972)]. The ADC8004 is capable to produce output 8 bits with corresponding input voltage starting from 0 to 2.5 voltages. As we are using 8-bit resolution output, which have 256 quantization levels, 1 to +127, 0 and -1 to -127.

**Table 1:** Shows Verification Test Result of ADC 0804 Encoder.

| Input Voltage (mV) | Quantization level | Output of ADC |
|---|---|---|
| 110 | +6 | 10000110 |
| 2530 | +127 | 11111111 |
| -710 | -36 | 00100100 |
| +930 | +47 | 10101111 |
| -550 | -28 | 00011100 |
| +270 | +14 | 10001110 |
| -2530 | -127 | 01111111 |

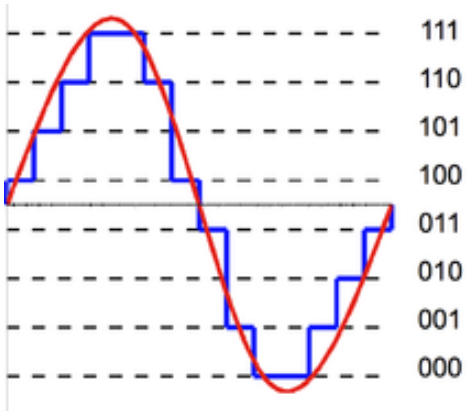


**Fig. 12:** Bit Quantization Level of Un-Uniform PCM System [17].

We have applied to the result of sequential voltage to digital output to in MATLAB. This is an actual result that shows uniform quantization characteristic of the encoder.

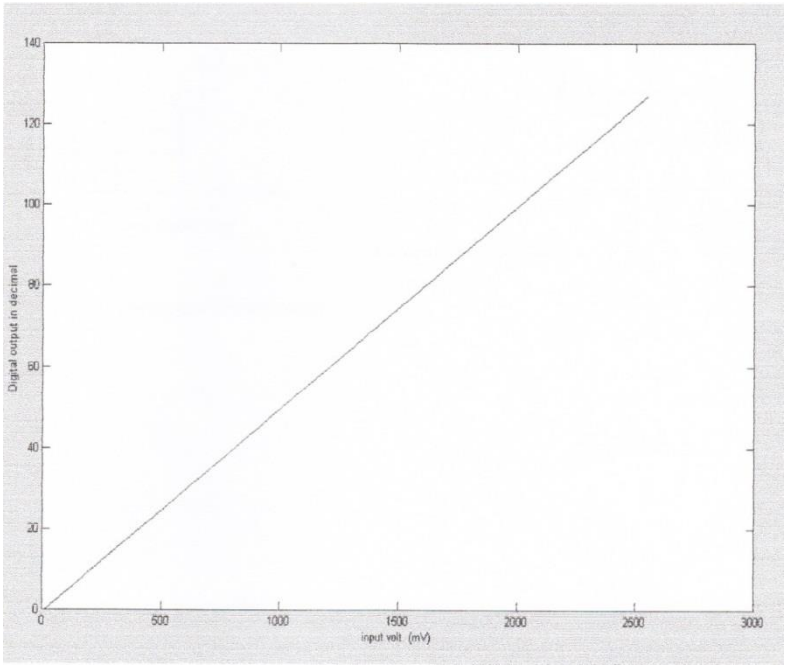


**Fig. 13:** Graphical Representation of the Quantization Characteristics.

## 5.2. Verification of hardware implementation of PCM system

The actual output (Table 2) of PCM system will be found after applying a voice signal to the system. We have applied a sinusoidal wave to the input of the sampler as an alternative voice signal source to prove the system. We have delayed the time of input frequency to see the change of conversation at the output end of ADC 0804 using LED in parallel of each bit. The finding of the result of the whole system is always similar to the result found applied to ADC 0804 individual. In the decoder side, it may differ with the original signal as our system is based on linear quantization.

**Table 2:** Shows Verification Test Result of Final Output of the System

| Input Voltage (mV) | Quantization level | Output of ADC | Final output of PCM system |
|---|---|---|---|
| 110 | +6 | 10000110 | 10000110 |
| 2530 | +127 | 11111111 | 11111111 |
| -710 | -36 | 00100100 | 00100100 |
| +930 | +47 | 10101111 | 10101111 |
| -550 | -28 | 00011100 | 00011100 |
| +270 | +14 | 10001110 | 10001110 |
| -2530 | -127 | 01111111 | 01111111 |

### 5.3. Digital to analogue converter

An analogue to digital Converter (ADC) obtains a digital value representing an input analogue voltage, while a digital to analogue (DAC) change a digital value back into analogue voltage. We have added this circuit to test how accurately the analogue signal gets back. A ladder networks are networks of resistors accepts inputs of binary value at 0 V to Vref and providing an output voltage proportional to input values. The figure shows a ladder network with 7 input voltages.

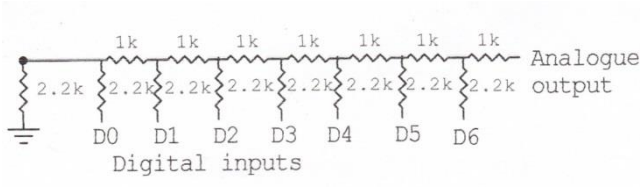


**Fig. 14:** Digital to Analogue Conversion Using Ladder Networks.

The output voltage is proportional to the digital input values as given by the relation:

$$v_{analog} = \frac{V_{ref.}(2^6.D_6 + 2^5.D_5 + 2^4.D_4 + 2^3.D_3 + 2^2.D_2 + 2^1.D_1 + D_0)}{2^8}$$

Di =0, or 1; where i=7,6,5,4,3,2,1,0. If D7=logic 1 then the number is +ve and of D7=logic 0 then the number is negative. Where Vref=Voltage for logic 1.
We have similar types of signal at the DAC output. The signal needs to filter to get original signal back.

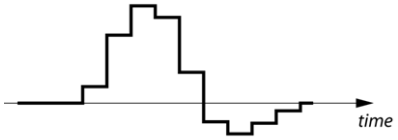


**Fig. 15:** Signal after Digital to Analogue Conversion.

### 5.4. Limitations

Our system is unable to use the concept companding to reduce quantization error as our ADC considers all value in a linear range to convert digital bits. However, companding is a process which can reduce quantization errors by considering the nonlinear quantization level at the lower range of frequency. Uniform quantization is not an optimum process to digitize as at low signal SNR is very small but high signal has large SNR. The SNR and quantization noise can affect voice quality. The more quantization the mere increase of communication bandwidth. Though we have implemented the PCM uniform manner, we believe the nonlinear quantization process is the best to execute in real time communication system. At the receiver end, expanding process helps to decode the original signal with having low quantization errors. We can solve our system by introducing nonlinear quantizer (Compressor) in between sample and hold circuit and ADC 0804.

## 6. Conclusion and future work

The study on hardware implementation of PCM proved techniques and importance of modulation techniques for some situation. We actually focused theory to practical implementation by which anyone can understand easily. Hardware implantation has some advantages over hardware-software such as time delay, cost, understanding, and execution. We have a future plan to develop to add a linear quantizer in between sample and hold and ADC of the system and want show comparative analysis with others. We want to implement both encoder and decoder in both μ-law and A-law modes with our system.

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