International Journal of Scientific World, 9 (2) (2023) 25-30

International Journal of Scientific World

Website: www.sciencepubco.com/index.php/IJSW

Research paper

Temperature-dependent short channel effects in nanoscale double gate FinFETs: A comparative study

Nura Muhammad Shehu [1] *, Garba Babaji [1], Mutari Hajara Ali [1]

[1] Department of Physics, Bayero University, Kano, Nigeria
**Corresponding author E-mail: hamnur2020@gmail.com*

Abstract

This work investigates the impact of temperature variation on Short Channel Effects (SCEs). Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN) and Silicon (Si) are the channel materials that are investigated. The study examines phenomenal metrics such as Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), Threshold Voltage Roll-off, On-current and Transconductance using PADRE Simulator. The results revealed that GaAs-FinFET excels in terms of DIBL, threshold voltage, transconductance and on-current at higher temperatures. On the other hand, GaN-FinFET excels in terms of SS at lower temperatures. These findings contribute to the understanding of temperature effects on nanoscale double gate FinFETs, aiding their optimization for diverse electronic devices.

Keywords: *Short Channel Effects; Temperature Variation; Double Gate; Channel Materials; DIBL; Subthreshold Swing.*

1. Introduction

Miniaturization is a remarkable journey undertaken by the semiconductor industry, which is driven by the desire to achieve better performance and efficiency through the reduction of semiconductor components ‘size [1], [2], [3]. The intriguing study of nanoscale transistors has resulted from this drive for downsizing. As we move farther into the area of diminishing technology nodes, the problem of shrinking transistor size becomes increasingly formidable [4], [5]. These restrictions occasioned by transistor downsize are referred to as Short Channel Effects (SCEs) [6], [7]. In an effort to get over these obstacles and continue the never-ending pursuit of advancement, researchers and engineers have turned their focus towards looking at alternative transistor architectures. Fin-Field Effect Transistors (FinFETs) on the other hand, are emerging as extremely promising alternative structures. They provide improved resilience to loss of dependability and have the potential to enable further scaling opportunities [8], [9], [10]. The current boom in finFET research is due to their several known benefits, such as the elimination of short channel effects [11]. As electronic devices get smaller and more powerful, variations in temperature emerge as a critical environmental component that can affect the SCEs in nanoscale Double Gate FinFETs.

In an effort to mitigate the adverse impacts of short channel effects (SCEs) in FinFETs, various researchers have conducted extensive investigations. Bhat et al. in [12] investigated the influence of short channel effects (SCEs) on the gate length and channel width of a double gate n-FinFET device utilizing various channel materials such as Si, GaAs, GaSb, and GaN. The results indicated that GaAs and GaN channel FinFETs outperformed Si and GaSb in terms of DIBL. GaN also outperformed GaAs for gate lengths smaller than 46nm. The study found that GaAs and GaN are promising channel materials for FinFET devices that can be used to minimize short channel effects and increase device performance. Roslan et al. [13] delved into the characteristics of Double Gate FinFETs and assessed how the physical parameters of FinFETs impact SCEs. Their research revealed desirable electrical attributes in double gate FinFETs, including high drive current and low off-state current. Chugh et al. [14] explored the influence of parameter variations on sub-50 nm finFETs, showcasing significant improvements for reduced gate lengths. Meanwhile, Shang et al. examined the impact of fin structure on 5 nm finFET technology, suggesting an optimal fin height of 50 to 60 nm. They noted that while a thinner fin improves DIBL performance, it also leads to an increase in threshold voltage due to the quantum confinement effect.

In a separate study, Roslan et al. [15] investigated the effects of a high-K material gate spacer on SCEs in double-gate FinFETs (DG-FinFETs), highlighting their advantageous electrical characteristics, such as high drive current and low leakage current. Kailasam & Govindasamy in [3] explored the electrical properties of DG-FinFETs by altering the gate dielectric materials, resulting in a substantial increase in transconductance and a significant decrease in leakage current when changing from SiO_2 to HfO_2. Huang et al. [16] employed a theoretical model to examine the impacts of Drain-Induced Barrier Lowering (DIBL) and short-channel effects in InGaAs negative-capacitance finFETs (NC-FinFETs). They found that strong negative capacitance effect can significantly reduce DIBL and subthreshold swing differences between InGaAs and Si FinFETs, particularly for gate lengths below 20 nm. However, the impact of temperature on short channel effects which plays a significant role in influencing the electrical properties of double gate FinFETs using Si, GaAs, GaSb and GaN as channel materials is yet to be investigated

Copyright © Nura Muhammad Shehu et al. This is an open access article distributed under the Creative Commons Attribution License, which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

The study investigated how temperature changes impact short channel effects in nanoscale double gate FinFETs using GaAs, GaSb, GaN, and Si as channel materials. The PADRE Simulator will be used to explore the phenomenal parameters DIBL, SS, threshold voltage roll-off, on-current, and transconductance.

1.1. Device structure

The device structure of an n-channel double gate FinFET is shown in Fig. 1. The structure has important parts such the source, drain, gate length (channel length), and channel width (fin width or fin thickness). Before making the gate contact, the oxide is placed on the top surface of the fin, both on the side walls, and both sides of the side walls. Tox1 and Tox2 are the oxide thickness of the side wall.

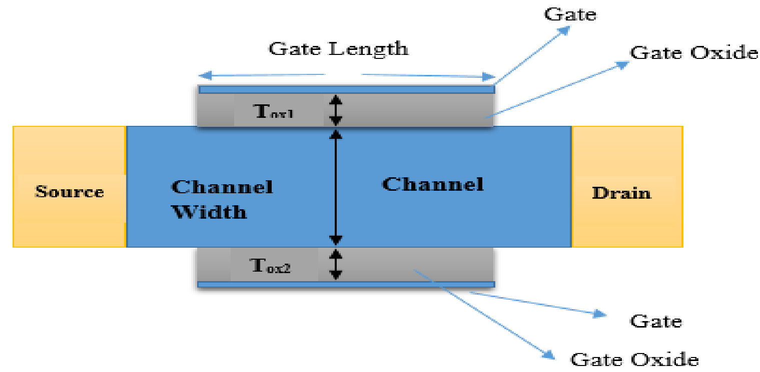

Fig. 1: Two-Dimensional Double Gate FinFET [17].

2. Method

We utilized the PADRE Simulator, a component of the Multigate Field Effect Transistors (MuGFET) tool, to perform simulations on our device. This simulator is proficient in generating informative curves that engineers can employ to characterize the underlying physics of Field Effect Transistors (FETs). Additionally, it provides consistent solutions to the equations of Poisson and drift-diffusion [18]. During the simulation, we explored the impact of varying temperature (ranging from 300K to 500K) on four distinct semiconductor materials: GaAs, GaSb, GaN, and Si, each employed as the channel material for the FinFETs. The simulation maintained a constant gate length of 45 nm and a channel width of 10 nm. The oxide thickness was set at 2 nm, while the channel doping concentration was held steady at 1×10^{16} cm^{-3}, and the drain/source at 1×10^{19} cm^{-3}. Our simulations involved drain biases ranging from 0.05 V to 1 V and gate biases spanning from 0 V to 1 V. The parameters are listed in Table 1.

Table 1: Parameter Specifications

Parameter	Value
Temperature	(300, 350, 400, 450, 500) K
Gate Length	45 nm
Oxide Thickness	2 nm
Channel Width	10 nm
Channel Doping Concentration	1×10^{16} cm^{-3}
Source/Drain Doping Concentration	1×10^{19} cm^{-3}
Drain Bias	0.05 V, 0.06 V, 1.0 V
Gate Bias	0V to 1.0 V

3. Results and discussion

The impact of temperature on short channel effects in nanoscale double gate FinFET devices using GaAs, GaSb, GaN and Si as channel materials is presented in this section. The important metrics delved into are DIBL, SS, Threshold Voltage Roll-off, On-current and Trans-conductance.

3.1. Impact of temperature variation on DIBL

The potential barrier is lowered when the drain voltage is raised, and this phenomenon is known as drain-induced barrier lowering (DIBL), one of the short channel effects. It may be computed for MuGFET devices as follows [19]:

$$\mathrm{DIBL}\left(\frac{\mathrm{mV}}{\mathrm{V}}\right) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \quad (1)$$

Where V_{TH} is denotes threshold voltage and V_{DS} denotes drain-source voltage.
Fig. 2 shows the findings of the drain-induced barrier lowering (DIBL) variation with regard to temperature.

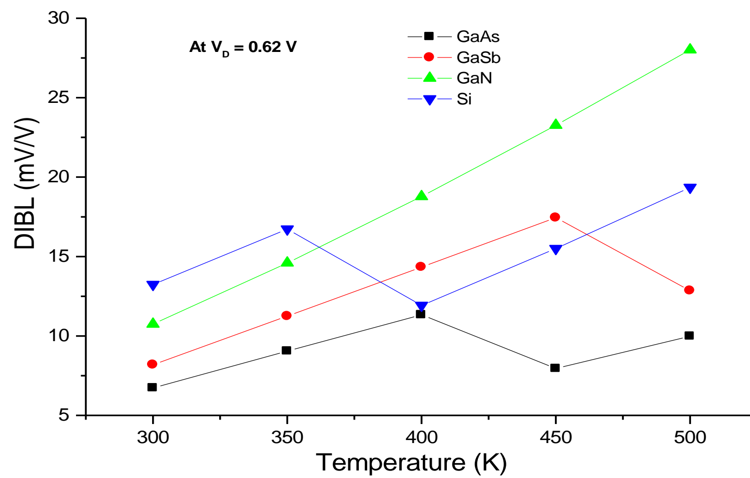

Fig. 2: DIBL vs Temperature.

As the temperature rises, the DIBL of GaN-FinFET increases. DIBL for Si-FinFET, on the other hand, rises from 300K to 350K and then falls at 400K, implying that 400K is the optimal operating temperature for this device. The DIBL of GaSb-FinFET increases from 300K to 450K, then decreases, with 500K acting as the optimal operating temperature. The DIBL of a GaAs-FinFET increases up to 400K, then reduces at temperatures over 400K until it reaches 450K, after which it rises again. GaAs-FinFET also performs better than the other FinFETs at 300K given that it has the lowest DIBL value, 6.73 mV/V. Reduced DIBL in FinFETs denotes improved control over the flow of current between the source and drain. This enhanced control results in more predictable and steady performance, which is critical for a variety of applications.

3.2. Impact of temperature variation on subthreshold swing

The subthreshold slope is an essential parameter in calculating the leakage current. As stated in [18], the following formula is used to calculate SS:

$$SS\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (log_{10}\ I_{DS}} \tag{2}$$

Where V_{GS} denotes the gate-source voltage and I_{DS} denotes the drain-source current.
Fig. 3 shows the impact of temperature on the subthreshold swing. The figure unequivocally shows that in all four of the finFETs under consideration, the subthreshold slope (SS) increases as the temperature rises. It is noteworthy that these devices work best at 300K, as lower SS is observed in them at this temperature. This decrease in SS causes a decrease in subthreshold current, which raises the devices' overall efficiency. It is clear that the subthreshold swing increases when the temperature rises above 300K, which is detrimental for the performance, power efficiency, and reliability of finFET devices.

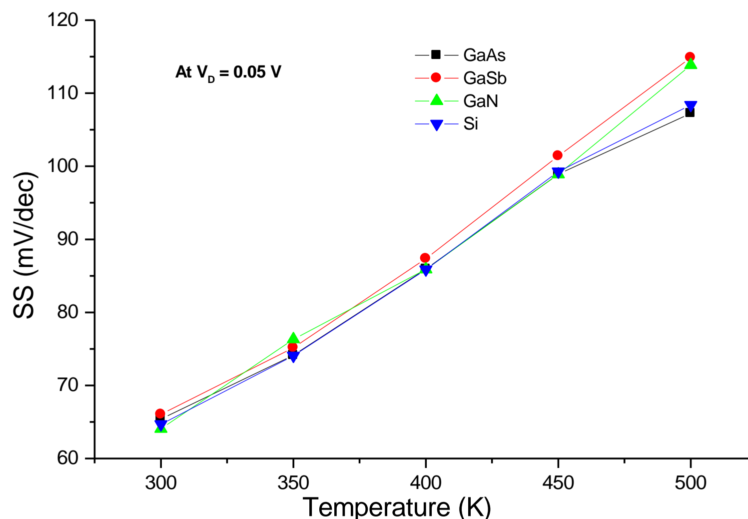

Fig. 3: SS vs Temperature.

3.3. Impact of temperature variation on threshold voltage

It is essential to perform a thorough evaluation of the device's threshold voltage in order to determine an appropriate channel material for a switching device [19]. The threshold voltage is the lowest gate voltage required to create a path between the source and drain [20]. In a multi-gate field-effect transistor (MuGFET) device, the expression for threshold voltage can be written as [21]:

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \tag{3}$$

Where Q_{SS} represents charge in the gate dielectric, C_{ox} denotes gate capacitance, Q_D is the depletion charge in the channel, f_{ms} represents metal semiconductor work function difference between gate electrode and the semiconductor, f_f denotes the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is needed for ultrathin body devices to bring enough inversion charges in to the channel region of the transistor to reach threshold point.
The impact of temperature on the threshold voltage of GaAs, GaSb, GaN, and Si-finFETs is shown in Fig. 4. The threshold voltages for all devices are found to fall as temperatures rise. The FinFET devices may benefit from this phenomena in a number of ways, including faster operation, less power usage, and more energy efficiency. GaAs-FinFET shows lowest threshold voltage at high temperature, which is 0.37 V. Si-FinFET, on the other hand, achieves the highest threshold voltage of 0.53 V at 300K. It's also important to note that in some circumstances, transistors with higher threshold voltages provide better long-term stability by minimizing deterioration brought on by things like hot carrier effects. Furthermore, finFETs with higher threshold voltage values can be seamlessly integrated into applications requiring compatibility with legacy semiconductor technologies or higher voltage levels within a system.

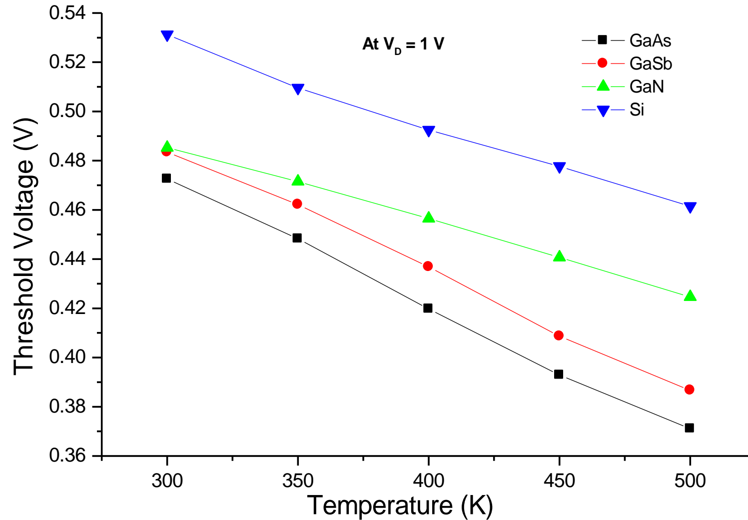

Fig. 4: Threshold Voltage vs Temperature.

3.4. Impact of temperature variation on current

Fig. 5 displays the outcomes regarding the variation of on-current with temperature. In GaSb, GaN, and Si finFETs, there is a noticeable decrease in on-current as temperature rises. This trend highlights that higher temperatures consistently lead to decreased on-current in these three finFETs. In contrast, the GaAs-finFET exhibits a distinct behavior, as its on-current increases consistently with rising temperature across the entire temperature range under consideration. This shows that GaAs is better than the other three FinFETs across the entire temperature range considered. FinFETs with greater on-current have better performance, energy efficiency, and adaptability, making them useful for a wide range of advanced semiconductor applications.

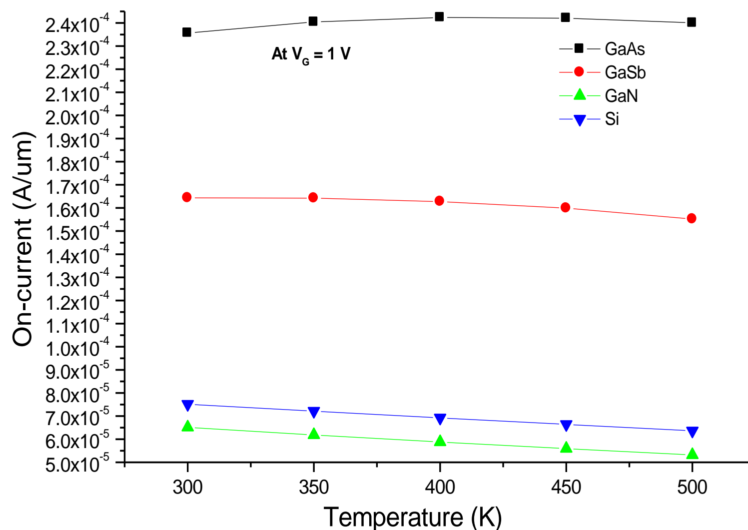

Fig. 5: On-Current vs Temperature.

3.5. Impact of temperature variation on transconductance

Transconductance, denoted as gm measures how the drain current changes with variations in the gate-source voltage while maintaining a constant drain-source voltage. It is calculated using [18]:

$$g_m = \frac{dI_D}{dV_{GS}} \qquad (4)$$

Where I_D is the drain current and V_{GS} is the gate-source voltage. Therefore, the value of gm is extracted by taking the derivative of the I_D-V_{GS} curve.
Fig. 6 shows how the transconductance of GaAs, GaSb, GaN, and Si FinFETs varies with temperature. Transconductance increases in all the four FinFETs as temperature rises, demonstrated by the figure. Notably, GaAs FinFETs have highest transconductance at 500K. This result indicates that all four FinFET types are capable of operating efficiently across the whole temperature range investigated, with their transconductance properties acceptable for a range of temperature-dependent applications. Lower supply voltage needs can result from higher transconductance, which in turn can lead to less power consumption, particularly with battery-powered devices like smartphones and Internet of Things (IoT) devices, lower supply voltages are crucial for power-efficient operation.

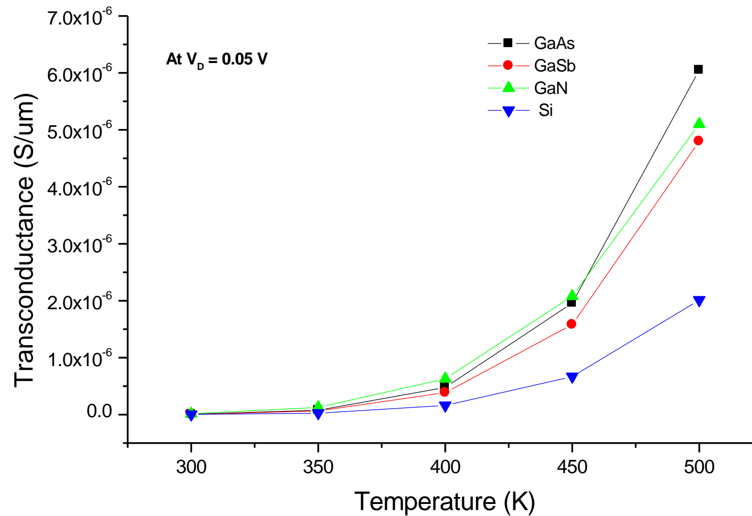

Fig. 6: Transconductance vs Temperature.

4. Conclusion

Temperature variations in nanoscale double gate FinFETs can worsen short channel effects, including threshold voltage shifts, increased subthreshold swing, and drain-induced barrier lowering, resulting in variations in performance and reliability issues. This work explored the influence of temperature variations on short channel effects (SCEs) in nanoscale double gate FinFETs employing diverse channel materials, including GaAs, GaSb, GaN and Si. The findings revealed that GaAs-FinFET excelled in terms of DIBL, threshold voltage, transconductance and on-current at higher temperatures. On the other hand, GaN-FinFET exhibited superiority in terms of SS at lower temperatures. These findings contribute valuable insights into the temperature effects on nanoscale double gate FinFETs, offering guidance for optimizing their performance in a wide range of electronic devices. Further research can be carried out to develop temperature compensation techniques or circuit designs to counteract the variations in threshold voltage and on-current observed with changing temperatures.

References

[1] Mahmood, W. A. Jabbar, Y. Hashim, and H. Bin Manap, "Effects of downscaling channel dimensions on electrical characteristics of InAs-FinFET transistor," *Int. J. Electr. Comput. Eng.*, vol. 9, no. 4, pp. 2902–2909, 2019, doi: 10.11591/ijece.v9i4.pp2902-2909. https://doi.org/10.11591/ijece.v9i4.pp2902-2909.

[2] H. Riel, L. Wernersson, M. Hong, and J. A. Alamo, "III – V compound semiconductor transistors — from planar to nanowire structures," *MRS Bulletin* 39, pp. 668–677, 2014, doi: 10.1557/mrs.2014.137. https://doi.org/10.1557/mrs.2014.137.

[3] M. Kailasam and M. Govindasamy, "Impact of high-k gate dielectrics on short channel effects of dg n-finfet," *Int. J. Sci. Technol. Res.*, vol. 9, no. 3, pp. 2023–2026, 2020.

[4] R. S. Rathore and A. K. Rana, "Investigation of metal-gate work-function variability in FinFET structures and implications for SRAM cell design," *Superlattices Microstruct.*, vol. 110, pp. 68–81, 2017, https://doi.org/10.1016/j.spmi.2017.09.003.

[5] M. Kalasapati and S. L. Tripathi, "Robustness evaluation of electrical characteristics of sub-22 nm FinFETs affected by physical variability," *Mater. Today Proc.*, vol. 49, pp. 2245–2252, 2021, https://doi.org/10.1016/j.matpr.2021.09.336.

[6] E. H. Minhaj, S. R. Esha, M. M. R. Adnan, and T. Dey, "Impact of Channel Length Reduction and Doping Variation on Multigate FinFETs," *2018 Int. Conf. Adv. Electr. Electron. Eng. ICAEEE 2018*, pp. 1–4, 2019, https://doi.org/10.1109/ICAEEE.2018.8642981.

[7] G. R. Murthy, S. Tiwari, and S. Marasu, "IMPACT OF DIELECTRIC MATERIALS ON FinFET CHARACTERISTICS AT 45nm USING SILVACO ATLAS 2-D SIMULATIONS," *Sci.Int.(Lahore)*, vol. 33, no. 1, pp. 61–64, 2021.

[8] Gopinadh and A. George, "Variation in Parameters on Electrical Characteristics of FinFET with High-k dielectric," *Int. J. Adv. Res. Electr. Electron. Instrum. Eng. (An ISO*, vol. 3297, pp. 8293–8299, 2007.

[9] N. El, B. Hadri, and S. Patanè, "Effects of High-k Dielectric Materials on Electrical Characteristics of DG n-FinFETs," *Int. J. Comput. Appl.*, vol. 139, no. 10, pp. 28–32, 2016, https://doi.org/10.5120/ijca2016909385.

[10] R. Saha, B. Bhowmick, and S. Baishya, "Deep insights into electrical parameters due to metal gate WFV for different gate oxide thickness in Si step FinFET," *Micro Nano Lett.*, vol. 14, no. 4, pp. 384–388, 2019, https://doi.org/10.1049/mnl.2018.5220.

[11] N. M. Shehu, M. H. Ali, and G. Babaji, "Performance Analysis of Nanoscale Double Gate Ge and GaSb finFETs," *Journ. of Sci. and Tech. Res.*, vol. 5, no. 2, pp. 322–330, 2023.

[12] T. A. Bhat, M. Mustafa, and M. R. Beigh, "Study of short channel effects in n-FinFET structure for Si, GaAs, GaSb and GaN channel materials," *J. Nano- Electron. Phys.*, vol. 7, no. 3, pp. 1–5, 2015.

A. F. Roslan *et al.*, "30nm DG-FinFET 3D construction impact towards short channel effects," *Indones. J. Electr. Eng. Comput. Sci.*, vol. 12, no. 3, pp. 1358–1365, 2018, https://doi.org/10.11591/ijeecs.v12.i3.pp1358-1365.

B. Chugh, V. Narula, S. Lata, and B. Raj, "The effects of variation in geometry parameters on sub-50 nm finfet and their direct impact on finfet performance," *Proc. - 2nd Int. Conf. Intell. Circuits Syst. ICICS 2018*, no. October, pp. 184–187, 2018, https://doi.org/10.1109/ICICS.2018.00045.

[13] F. Roslan *et al.*, “Comparative high-K material gate spacer impact in DG-finfet parameter variations between two structures,” *Indones. J. Electr. Eng. Comput. Sci.*, vol. 14, no. 2, pp. 573–580, 2019, https://doi.org/10.11591/ijeecs.v14.i2.pp573-580.

[14] S. E. Huang, W. X. You, and P. Su, “Mitigating DIBL and Short-Channel Effects for III-V FinFETs with Negative-Capacitance Effects,” *IEEE J. Electron Devices Soc.*, vol. 10, pp. 65–71, 2022, https://doi.org/10.1109/JEDS.2021.3133453.

A. S. C. & S. M. M. A. M. Md. Javed Hossain, “Impacts of Variations in Channel Length, Width and Gate Work Function of Gan FinFET and Si-FinFET on Essential Electrical Parameters,” *Int. J. Electr. Electron. Eng. Res.*, vol. 9, no. 2, pp. 29–42, 2019, [Online]. Available: http://www.tjprc.org/publishpapers/2-15-1572850801-4.IJEEERDEC20194.pdf.

[15] S. I. et al. . Shafiqul Islam et al., “A Comparative Study of Sub-10nm Si, Ge and GaAs n-Channel FinFET,” *Int. J. Semicond. Sci. Technol.*, vol. 7, no. 1, pp. 1–6, 2017, https://doi.org/10.24247/ijsstdec20171.

[16] M. S. Islam, M. S. Hasan, M. R. Islam, A. Iskanderani, I. M. Mehedi, and M. T. Hasan, “Impact of Channel Thickness on the Performance of GaAs and GaSb DG-JLMOSFETs: An Atomistic Tight Binding based Evaluation,” *IEEE Access*, vol. 9, pp. 117649–117659, 2021, https://doi.org/10.1109/ACCESS.2021.3106141.

[17] S. Banerjee, E. Sarkar, and A. Mukherjee, “Effect of Fin Width and Fin Height on Threshold Voltage for Tripple Gate Rectangular FinFET,” *TTIC,* vol. 2, pp. 27–30, 2018.

[18] M. Mustafa, T. A. Bhat, and M. R. Beigh, “Threshold Voltage Sensitivity to Metal Gate Work-Function Based Performance Evaluation of Double-Gate n-FinFET Structures for LSTP Technology,” *World J. Nano Sci. Eng.*, vol. 03, no. 01, pp. 17–22, 2013, https://doi.org/10.4236/wjnse.2013.31003.