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Research paper

Optimizing dielectric constants for enhanced performance in nanoscale DG-FinFETs: A comprehensive study on short channel effects

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Abstract

This study explores how variations in fin and gate dielectric constants impact nanoscale, DG-FinFETs' sensitivity to Short Channel Effects (SCEs). Various fin (channel) materials; Gallium Arsenide (GaAs), Gallium Antimonide (GaSb), Gallium Nitride (GaN), and Silicon (Si), are considered. PADRE simulation environment is used to investigate the threshold Voltage (Vth) Roll-off, a crucial performance parameter. GaAs-FinFET, with a gate dielectric and fin dielectric constant values of 15 and 45 shows the lowest threshold voltage of 0.412 V. The study concludes that FinFETs with a higher fin dielectric constant than gate dielectric constant exhibit reduced SCEs, leading to lower power consumption, faster switching, and improved efficiency. This underscores the importance of optimizing dielectric constants, especially the fin dielectric constant, for enhanced DG-FinFET performance.

Keywords: *DG-FinFETs; Dielectric Constant; Efficiency; PADRE; Short Channel Effects; Threshold Voltage.*

1. Introduction

As semiconductor technology progresses to nanoscale levels, the design and optimization of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) becomes substantially important in meeting the needs of contemporary electronics; improved performance and efficiency [1-6]. However, (SCEs) [7-8] present serious challenges that can undermine the efficiency and reliability of devices as their dimensions decrease. Nanoscale Double Gate FinFET (DG-FinFET), one of the new transistor topologies, has gained researchers' substantial interest because of the potential for better performance, reduced SCEs and scalability [9-12]. In this scenario, optimizing nanoscale DG-FinFET performance is critical. One major approach to achieve this optimization is to strategically manipulate fin (channel) and gate dielectric constants, which have a direct impact on device characteristics such as threshold voltage, subthreshold swing, and transconductance. By systematically varying the fin and gate dielectric constants, it is possible to identify optimum points that can enhance device performance metrics while maintaining the lowest possible threshold voltage.

An extensive literature review has yielded important insights that have led to our current investigation. In order to address SCEs, authors in [13] replaced silicon dioxide with zirconium oxide as the gate dielectric having higher dielectric constant. This replacement reduced the leakage current in FinFETs which led to the improvement in the device performance. Comprehensive research has been undertaken in [14] to improve FinFET performance and extend CMOS-based technology. The findings revealed that when compared to other gate dielectric materials, La_2O_3 gate dielectric, among other high-k materials, demonstrated considerable increases in transconductance, threshold voltage, reduced SCEs, and overall FinFET performance. In [15], the electrical properties of double gate Fin-FETs were studied using a variety of gate dielectric materials. The authors replaced Silicon-di-Oxide (SiO_2) with Hafnium Oxide (HfO_2) was substituted as gate dielectric material, the device's leakage current decreased significantly. The authors concluded that compared to other gate dielectric materials like SiO_2, HfO_2 performed better in double gate FinFETs. The SCEs of various dielectric constants such as SiO_2 and other high-k dielectric materials such as Si_3N_4, Al_2O_3, ZrO_2 and HfO_2 were investigated in [16]. The authors established that HfO_2, among the dielectric materials examined, exhibited excellent characteristics since its SCEs were lower than those of the other materials. In [17] , SiO_2 was replaced by a high-k dielectric material, HfO_2. The researchers demonstrated that HfO_2 had fewer SCEs than typical SiO_2, including a lower threshold voltage and off-state leakage current, implying that HfO_2 might be used as a novel dielectric material to mitigate SCEs. However, there exists a need to investigate how simultaneous variations in the fin and gate dielectric constants can affect the susceptibility of nanoscale DG-FinFETs to short channel effects.

This work seeks to explore how simultaneous variations in the fin and gate dielectric constants can affect the sensitivity of nanoscale DG-FinFETs to short channel effects using GaAs, GaSb, GaN and Si as fin materials. Threshold voltage is the main parameter upon which the performance of the device will be investigated using PADRE Simulator.

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2. Theoretical background

This section discusses the FinFET device structure, Short Channel Effects and FinFET terminologies.

2.1. FinFET device structure

A kind of metal oxide semiconductor field effect transistor known as a finFET is a multi-gate MOSFET. Chenming Hu and his associates created it for the first time in 1998 at the University of Berkley in California [24]. The FinFET is characterized by its conducting channel being encircled by a thin silicon "fin" that serves as the device's body. The thickness of the device determines its channel length. [4]. The distance between the source and drain junctions of a MOSFET is referred to as its channel length. The FinFET is a non-planar, double-gate transistor that is built on bulk silicon-on-insulator (SOI) or silicon wafers. [18]. Double Gate FinFET is shown in Fig. 1.

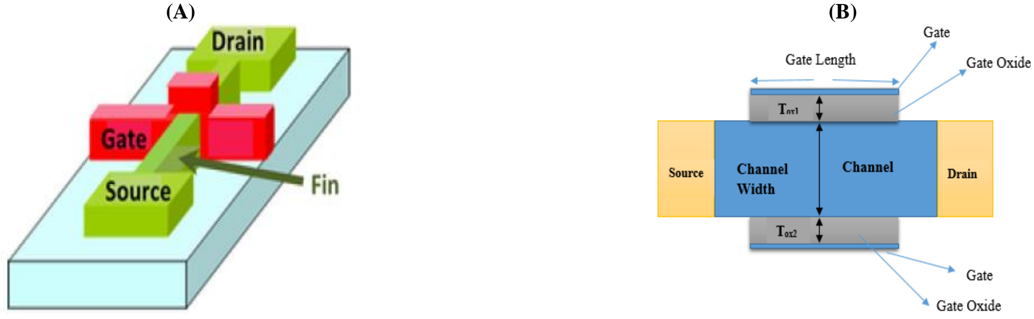

Fig. 1: (A) and (B): Double Gate FinFET Structure [4], [19].

The basic idea behind the FinFET construction is to bring the gate capacitance near FinFET channel. The fin body is typically quite narrow, giving the gate superior control over the channel. To accomplish this, the silicon body is very thin, ensuring that no leakage path is too distant from one of the gates, hence lowering leakage current. Because the channel is regulated by two or more gates, they provide more control over the channel [18].

2.2. Short channel effects and FinFET terminologies

Scaling down MOSFETs introduces issues that lead to performance deterioration. These issues are known as Short Channel Effects. Short Channel Effects and FinFET terminology include the following:

1) Drain Induced Barrier Lowering (DIBL)

The increase in drain voltage from 0.01 V to 0.05 V causes a variation in threshold voltage. This is referred to as drain induced barrier lowering. It is one of the most critical short channel effects. The DIBL value can be determined using [20]:

$$\mathrm{DIBL}\left(\frac{mV}{V}\right) = \frac{\Delta V_{TH}}{\Delta V_{DS}} \tag{1}$$

Where V_{TH} denotes threshold voltage and V_{DS} denotes drain-source voltage.

2) Subthreshold Swing

The subthreshold swing parameter, one of the SCEs, for a Multigate Field Effect Transistor is usually 60 mV/dec. The SS can be calculated by [14]:

$$\mathrm{SS}\ (mV/\ dec) = \frac{d\ V_{GS}}{d\ (\log_{10}\ I_{DS})} \tag{1}$$

Where V_{GS} denotes gate-source voltage and I_{DS} denotes drain-source current.

3) Threshold voltage

Assessing the threshold voltage of a device is a crucial step in determining its feasibility as a channel material for switching applications. The lowest gate voltage required to provide a conduction path between the source and the drain is known as the threshold voltage. [21]. The threshold voltage of a FinFET device can be calculated using [3]

$$V_{th} = f_{ms} + 2f_f + \frac{Q_D}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} + V_{in} \tag{3}$$

Where Q_{SS} denotes charge in the gate dielectric, C_{ox} is the gate capacitance, Q_D is the depletion charge in the channel, f_{ms} denotes metal semiconductor work function difference between gate electrode and the semiconductor, f_f is the fermi potential, and V_{in} is the additional surface potential to $2f_f$ that is needed for ultrathin body devices to bring enough inversion charges in to the channel region of the transistor to reach threshold point [3].

4) Transconductance

Transconductance is one of the important performance parameters for FinFET devices. While maintaining a fixed drain-source voltage, the transconductance quantifies how the drain current changes in response to variations in the gate-source voltage. This parameter can be calculated using [22]:

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4}$$

Where I_D denotes the drain current and V_{GS} denotes the gate-source voltage.

5) Parallel plate capacitor

If a FinFET is modelled as parallel plate capacitor, the capacitance of the device rises by a relative dielectric constant, k, when a dielectric material is placed between the metal gate and the semiconductor material. This capacitance is given by [23]:

$$C_{ox} = \frac{k\varepsilon_0 A}{t_{ox}} \quad (5)$$

Where C_{ox} is the gate capacitance, k is the dielectric constant of the material, ε_0 is the permittivity of free space, t_{ox} is the thickness of dielectric layer.

3. Materials and method

This section describes the materials and the method that were used during the device simulation.

3.1. Materials

The materials used in this research are Si, GaAs, GaSb and GaN as fin (channel) materials, silicon dioxide (SiO_2) as the gate dielectric, Silicon as base substrate and MuGFET simulation tool.

3.2. Method

The FinFET device was simulated using a PADRE Simulator, which is a part of the Multigate Field Effect Transistors (MuGFET) tool. Engineers may use this simulator to generate crucial curves that describe the basic physics of Field Effect Transistors (FETs). [22]. Furthermore, it yields consistent solutions for the Poisson and drift-diffusion equations. During the simulation, the effect of simultaneously varying the gate dielectric and fin (channel) dielectric constants both ranging from 15 to 45 was investigated utilizing GaAs, GaSb, GaN, and Si as the fin (channel) materials for the FinFET. A fixed gate length of 45 nm and channel width of 10 nm were maintained. The oxide thickness was set at 2 nm, while the channel doping concentration was held steady at 1×10^{16} cm^{-3}, and the drain/source doping concentration at 1×10^{19} cm^{-3}. The set drain bias ranged from 0.05 V to 1 V and gate bias ranged from 0 V to 1 V.

4. Results and discussion

This section presents and analyzes the findings of simulations that investigated how simultaneous variations in the fin and gate dielectric constants impact the susceptibility of nanoscale DG-FinFETs to short channel effects utilizing GaAs, GaSb, GaN, and Si as fin materials. Threshold voltage is the major parameter used to investigate the device's performance.

4.1. Threshold voltage at the gate dielectric constant of 15 and fin dielectric constant of 15 to 45

Fig. 1 presents the simulation results obtained of threshold voltage characteristics by varying the fin (channel) dielectric constant from 15 to 45 while maintaining a fixed gate dielectric constant of 15 for nanoscale DG GaAs, GaSb, GaN and Si FinFETs. Fig. 1 shows that the threshold voltage in GaN and Si GaAs decreases with increasing fin dielectric constants. GaSb and GaN have comparable threshold voltage behaviors between fin dielectric constants of 15 and 35, indicating potential interchangeability. However, GaSb-FinFET threshold voltage rises from 35 to 40 and then stabilizes. In contrast, GaAs-FinFET demonstrates a substantial fall in threshold voltage with a fin dielectric constant of 45, attaining the lowest value of 0.412 V among all FinFETs simulated. This demonstrates GaAs-FinFET's superior performance in terms of lower power consumption as well as faster switching speed, particularly for gate and fin dielectric constants of 15 and 45, (15, 45). This modelled FinFET has faster switching speed than the ones by [14] and [7] as the threshold voltage obtained in this work is lower. This makes the DG-FinFET in this work more immune to SCEs.

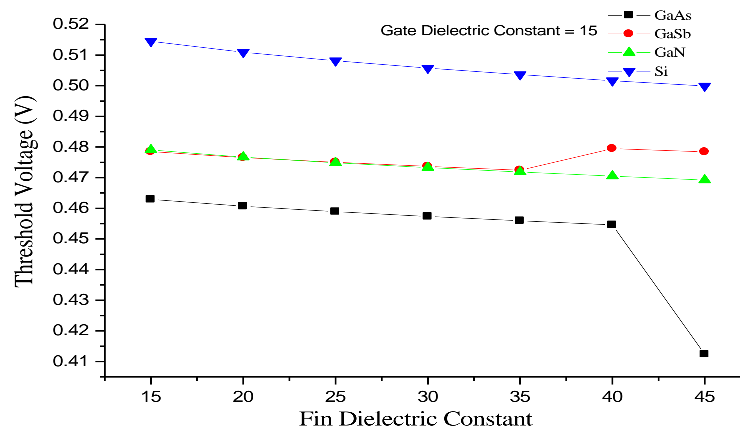

Fig. 1: Threshold Voltage vs Gate Fin Dielectric Constant at Gate Dielectric Constant of 15.

4.2. Threshold voltage at the gate dielectric constant of 20 and 25 and fin dielectric constant of 15 to 45

Fig. 2 and 3 show the simulation results of threshold voltage characteristics for nanoscale DG GaAs, GaSb, GaN, and Si FinFETs, where the fin dielectric constant ranges from 15 to 45 and the gate dielectric constant remains constant at 15 (Fig. 2) and 20 (Fig. 3). In all four FinFETs, increasing fin dielectric constants results in lower threshold voltages. Notably, GaAs-FinFET shows a considerable decline in

threshold voltage with a fin dielectric constant of 45, achieving the lowest value of 0.454 V among the simulated FinFETs the at gate and fin dielectric constants of 20 and 45 (20, 45) in Fig. 2; 25 and 45 (25, 45) in Fig. 3.

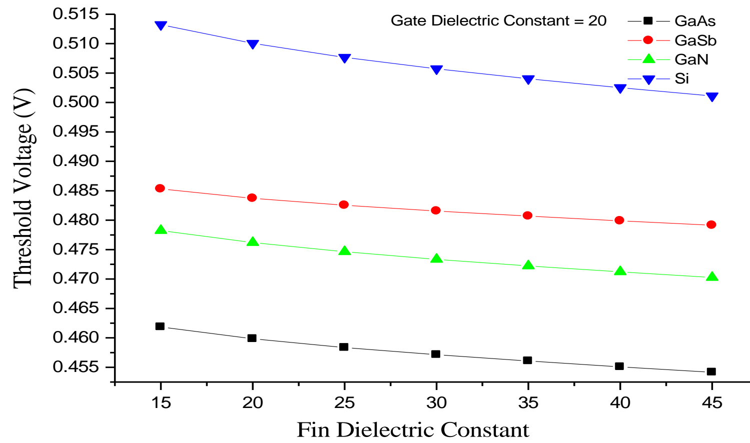

Fig. 2: Threshold Voltage vs Fin Dielectric Constant at Gate Dielectric Constant of 20.

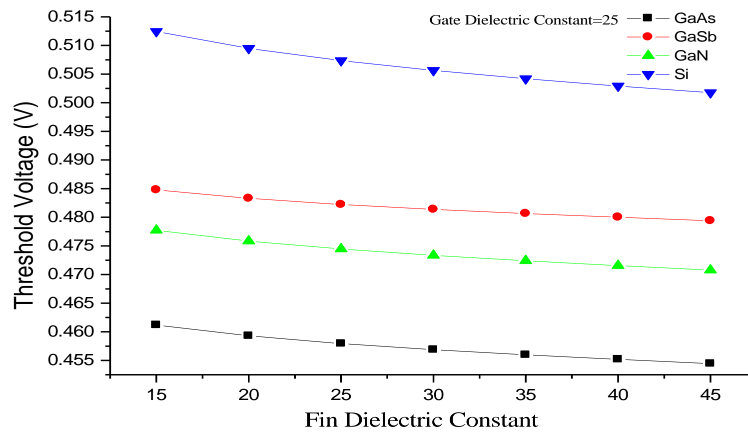

Fig. 3: Threshold Voltage vs Fin Dielectric Constant at Gate Dielectric Constant of 25.

4.3. Threshold voltage at the gate dielectric constant of 30 to 45 and fin dielectric constant of 15 to 45

The simulation results obtained for threshold voltage in nanoscale DG GaAs, GaSb, GaN and Si FinFETs are presented in Fig. 4, 5, 6 and 7 and discussed here. In Fig. 4, 5, 6, and 7, the threshold voltages of four FinFETs decrease as the fin dielectric constant increases from 15 to 45, while maintaining gate dielectric constants of 30, 35, 40, and 45, as illustrated. However, in Fig. 5 GaSb-FinFET shows an exception, where the threshold voltage rises from 0.484 V to 0.498 V as the fin dielectric constant increases from 15 to 20, with a fixed gate dielectric constant of 35. Across all four figures, GaAs-FinFET consistently exhibits the lowest threshold voltage of 0.455 V at gate dielectric constants of 30, 35, 40, 45 and fixed fin dielectric constant of 45, (30, 45) in Fig. 4, (35, 45) in Fig. 5, (40, 45) in Fig. 6, and (45, 45) in Fig. 7 respectively, in comparison to the other three FinFETs. The consistent decrease in threshold voltage across various gate dielectric constants suggests that increasing the fin dielectric constant enhances the overall performance of FinFET devices.

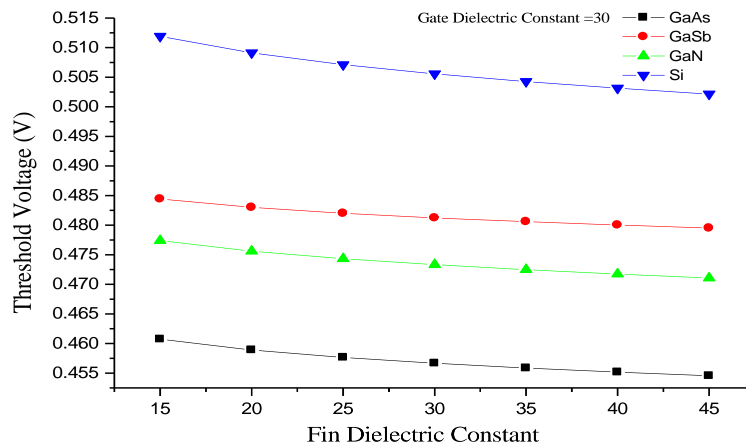

Fig. 4: Threshold Voltage vs Fin Dielectric Constant at Gate Dielectric Constant of 30.

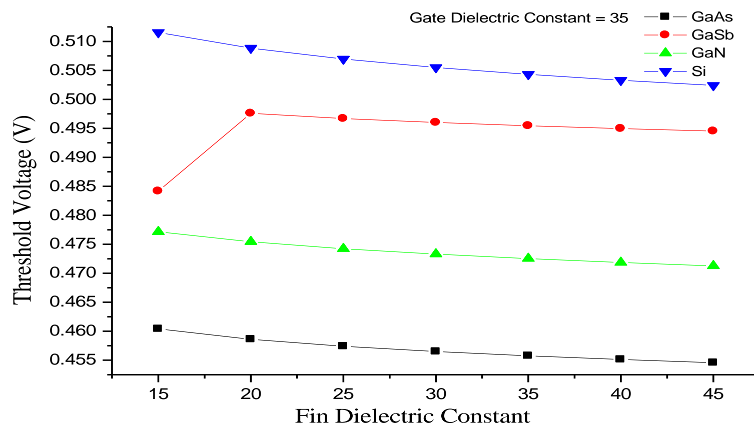

Fig. 5: Threshold Voltage vs Fin Dielectric Constant at Gate Dielectric Constant of 35.

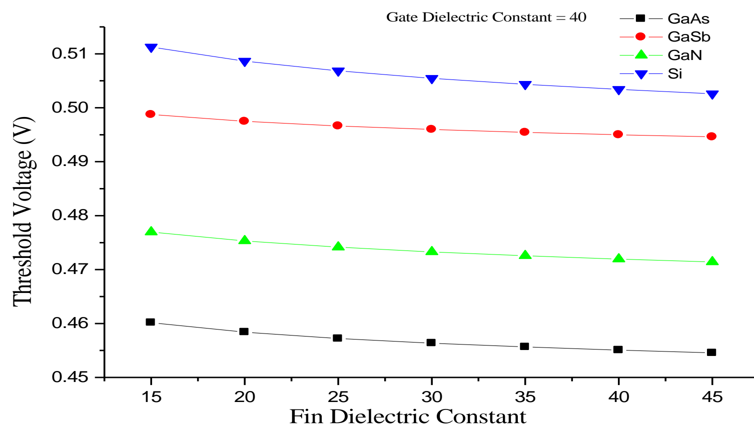

Fig. 6: Threshold Voltage vs Fin Dielectric Constant at Gate Dielectric Constant of 40.

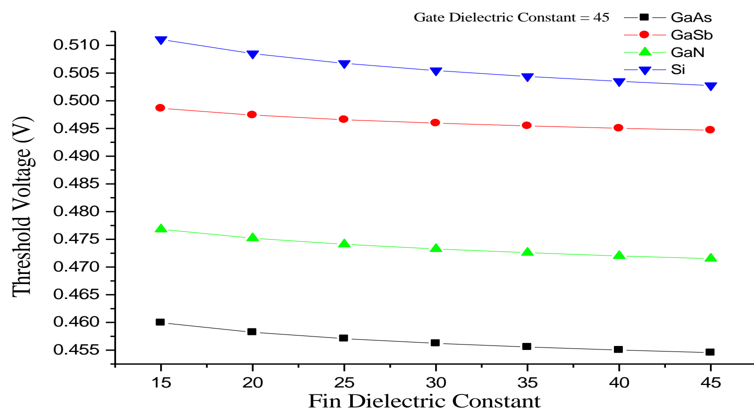

Fig. 7: Threshold Voltage vs Fin Dielectric Constant at Gate Dielectric Constant of 45.

5. Conclusion

In conclusion, this research extensively explored the influence of simultaneous variations in fin and gate dielectric constants on the sensitivity of nanoscale DG-FinFETs to short channel effects, utilizing GaAs, GaSb, GaN, and Si as fin materials. The primary focus of the study was on the threshold voltage as a key parameter for assessing device performance. The results demonstrated a notable impact of varying the fin dielectric constant while fixing the gate dielectric constant on the threshold voltage of the DG-FinFETs. Across various gate dielectric constant values, an increase in the fin dielectric constant generally correlated with lower threshold voltages for all four FinFETs. Notably, GaAs-FinFET exhibited the lowest threshold voltage at a high fin dielectric constant and low gate dielectric constant. In summary, FinFET devices with a higher fin dielectric constant than gate dielectric constant showed a consistent trend of reduced short channel effects. This reduction can lead to benefits such as lower power consumption, faster switching speed, and enhanced overall device efficiency. The study underscores the critical importance of optimizing dielectric constants, particularly the fin dielectric constant, to effectively mitigate short channel effects and elevate the performance of nanoscale DG-FinFETs. Future research directions may involve exploring additional fin materials, investigating the impact of other device parameters on short channel effects, and optimizing the fabrication process to achieve even more robust device performance.

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