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Research Paper

Design and comparative analysis of inexact speculative adder and multiplier

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Abstract

A Carry look ahead adder is a sort of the summer used in the logic design of the digital systems. The CLA boost up the speed by decreasing the measure of duration needed to calculate the carry bits. The CLA based outline of the inexact speculative adder is pipelined architecture to incorporate couple of logic paths along its basic way and in this manner, improving the recurrence of operation. This paper presents the comparative analysis of the pipelined inexact speculative adder and the general carry look ahead adder and showed that the delay is reduced to 48.27% when compared to carry look ahead adder and also we have designed the pipelined multiplier using the Inexact speculative adders and observed that the delay is reduced to 48.32% when compared to the normal multiplier. This entail Xilinx ISE Design Suite 14.5 Tool.

Keywords: *Inexact Speculative Adder, Multiplier, Carry Look Ahead Adder, Pipelining, Delay.*

1. Introduction

The inexact speculative adder is designed in such a way that the carry propagation chain is splitted into multiple paths which are concurrently executed. Each path again contains a error compensation block, sub-adder block and a carry speculator block. The partial signal is generated by the speculator block and to give the local sum the sub adder block uses carry in. Faulty sums are corrected by the compensation block which corrects either local sum or reduces the magnitude in the error. The carry for speculation block is generated by using the bits in carry look ahead sourced either by dynamic or static input. Errors are distributed evenly by the latter in ETBA. Speculation faults are detected by the COMP block by comparing carry out and generated carry from the speculation block. The COMP block is implemented between ADD blocks. The addition is implemented by following five steps mainly. First for each sub-adder block , a carry-in is speculated from short carry propagation chain and next based on that carry in local sum is calculated by the sub adder. Faulty speculation is detected by comparing the carry in and the carry out of the sub adder. Correction of local sum is done when there is wrong speculation. Error magnitude is minimized by the balance of preceding sum bits if the correction is not possible. The inconsistency between expected carry and speculated carry is detected by the COMP block by using the XOR gate because of which error flag is created that triggers activation either error reduction or correction compensation techniques. The three main advantages of this technique is that optimization of block size, speculation and correction trade-off and error minimization and failed correction [1].

In the speculative addition with the variable latency CSPA block has carry and adder circuits. Carry predictor helps in prediction of carry out bit. And adder has three internal components namely multiplexer which consists of multi bit, the sum generator and also an internal carry generator. Carry out bit of the adder block is predicted by the carry predictor. Internal signals to be used in the sum generator are produced by the internal carry signals. Multiplexer takes the input from the carry predictor and selects on of the carry signals. Sum generator calculates the partial sum bits of adder block. The proposed method works as follows, internal carry generators and predictors work simultaneously when input patterns arrive. The carry out bit of the predictor is given to next block adder and it is the selector for multiplexer and next internal carry signal is determined and is sent to the sum generator. Error recovery and detection circuit is also used. Error signal is 0 when there is no error and valid signal becomes 1 when an error occurs error and valid signal becomes vice versa during error input registers becomes disable and no input is taken [2].

The carry speculative adder with modification of carry generators that uses only less number of gates. In order to get data continuously into circuit the data latching circuit is used. To get results accurately the error recovery and detection circuit is included. The CSPA is implemented in a way that in the modified adder block sum and carry generators are separated by an logic which results in increase of area and consumption of power. To minimize the area two carry generators are for carry in=1 and carry in=0 used instead of one. AND gate is replaced in the place of 1bit carry generator for carry in=1 and carry in=0 it is replaced with OR gate. Two types of modified carry generators are used in place of two carry generators which has one gate delay with very less area.

These generators produce carry without using Cin bit. In the design of variable latency CSPA the circuits such as error recovery, error detection, data latching are used [3]. When the input is received the output sum is given by the circuit (VLCSPA). Error block signals and error signals is given by the error detection circuit. Multiplexer which is multibit takes the input from the recovery circuit and cspa when it is 1 signal recovery is from recovery circuit and when it is 0 result is selected from CSPA. Input registers become disabled when an error occurs and no input is taken and XOR gate is used in place of not gate and ex-or operation is used between error signal and its compliment.

2. Proposed Inexact Speculative Adder

There are many drawbacks in adders such as high area, high path delay and very high power consumption. To overcome all these problems speculative adders are implemented which has both techniques of speculation and correction that helps in achieving low power, high speed and area efficient design when compares with the existing adders. The inexact speculative adder consists of blocks they are adder, speculator and compensator as shown in the Fig.1 [4].

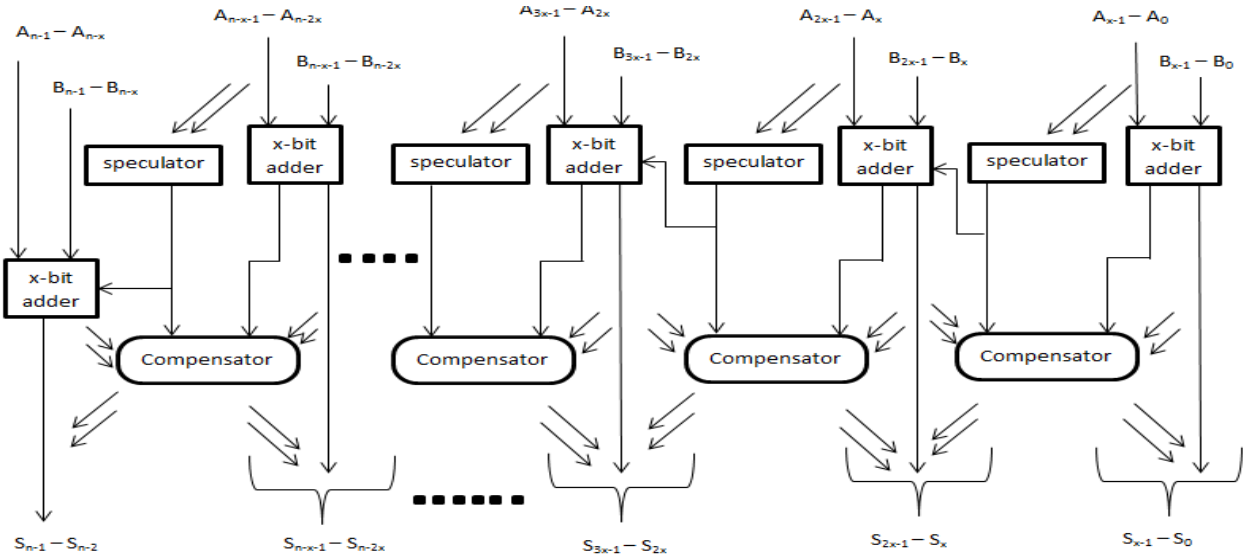

Fig. 1: General Block diagram of inexact speculative adder

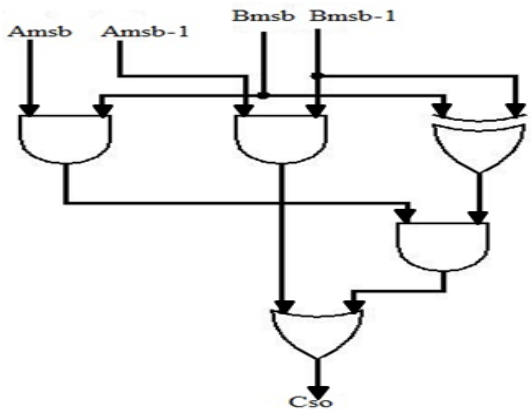

Fig. 2: Logic level representation of speculator

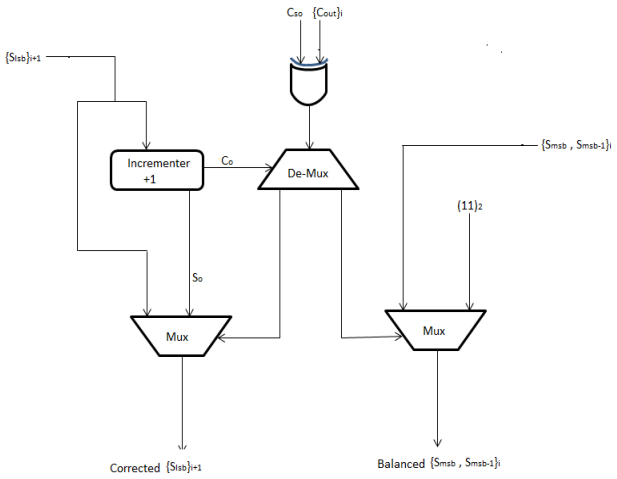

Fig. 3: Implementation of the compensator block

A. About Adder And Speculator

Two n- bit operands for the addition are represented by A= $A_0,A_1,A_2,.....A_{n-1}$ and B= $B_0,B_1,B_2,.....B_{n-1}$ and the carry in , carry out and sum is represented by C_{in} , C_{out} and S=$S_0,S_1,S_2,....S_{n-1}$ respectively. The output carry which is denoted C_o from each speculator as shown in the Fig.2 [4] is given as the input carry for each adder block subsequent to it. The adder block evaluates the sum based on the equation given below.

$$S_i = P_i \oplus C_i \quad (1)$$

The speculator block evaluates the carry based on the equations given below.

$$G_i = A_i \,.\, B_i \quad (2)$$

$$P_i = A_i \oplus B_i \quad (3)$$

$$C_{i+1} = P_i.C_i + G_i \quad (4)$$

Where P_i represents the carry propagate and G_i represents the carry generate.

B. About Compensator

This block compares the output carry from each adder block with the corresponding speculated carry using the xor gate. If the output of xor gate is zero then the sum is directly passed through the final output. Identically, if the xor gate output is one then it specify that error has been occurred which may be either positive or negative. The positive error specify the speculation of zero instead of one had occurred and indicates too low sum. The negative error specifies the speculation of one instead of zero had occurred and indicates too high sum. The compensator block carry out the unsigned accretion and depletion to the cluster of LSBs in this way the too high error is solved by a -1 and too low by a +1. In case of the overflow, the compensator block equalizes a cluster of MSBs of the predating adder in the opposite direction of the error as shown in the Fig 3 [1][4].

3. Design Methodology

The pipelined architecture of inexact speculative adder reduces the delay and gives the high speed. So as shown in the Fig.4 [4] it comprises of three main blocks they are pipelined speculator, pipelined carry look ahead adder and the pipelined compensator

for 16 bit addition. Pipelined CLA of 4 bits is used here. For the first pipelined is given the carry in and for the succeeding ones the output carry from the pipelined speculator is given. It consists of five pipelined stages for the achievement of speed. The pipelined CLA is shown in the Fig. 5 has one pipelined stage with the inputs A_0-A_4 and B_0-B_4 and the C_{in} and outputs are C_{out} and S_0-S_4 respectively. And now Coming to the pipelined compensator of pipelined stage comprises of the multiplexer, incrementor and the de-multiplexer as shown in the Fig.6 [1],[4].

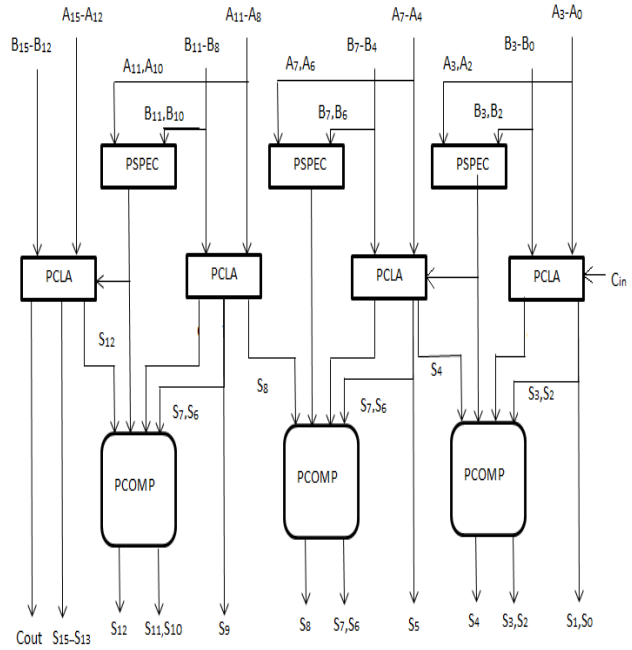

Fig. 4: Pipelined inexact speculative adder

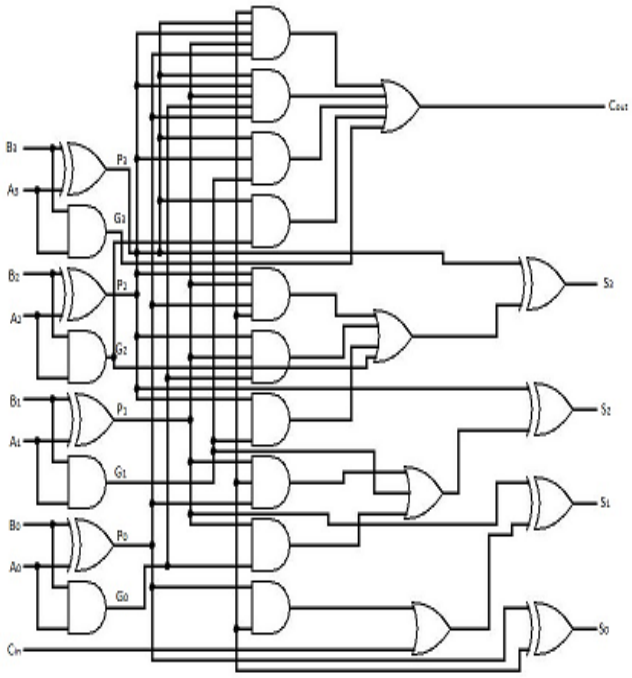

Fig. 5: Pipelined carry look ahead adder of four bits

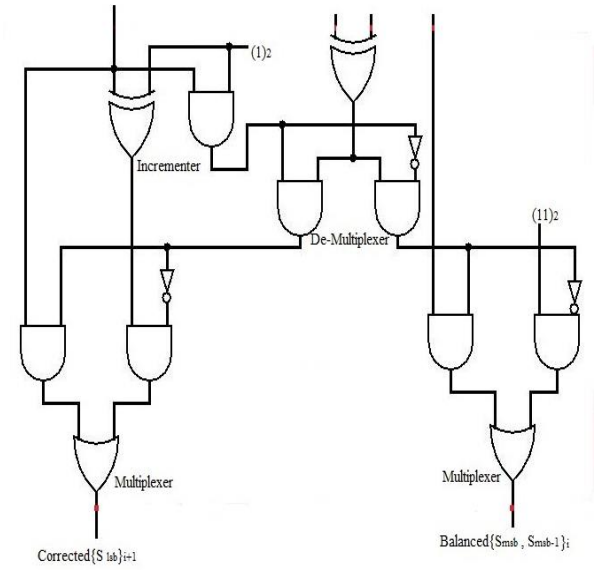

Fig. 6: Logic level of the pipelined compensator

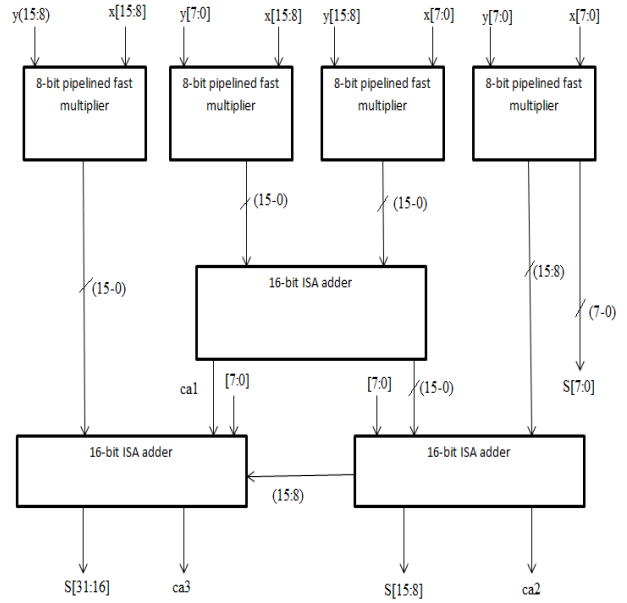

Fig. 7: Pipelined fast multiplier of 16-bit using ISA adders

As we know that the multiplication is fundamental building block of many digital designs there is need of having the multipliers that achieve the high speed and the low power. So one of the method is the use of The speculative multiplier can be done by using the methods such as carry-save tree and the carry speculation compression and by carry-save reduction tree have been explained in the literature [5]-[7]. Here we have designed the pipelined fast multiplier using the ISA adders of 16-bits using the 8-bit pipelined fast multiplier and 16-bit ISA adders. By using this method, we have achieved the high speed and reduced the delay.

4. Simulation Results and Tables

The Fig.8 shows the output of the pipelined 16 bit inexact speculative adder based CLA for the given inputs A,B,C_{in} and gives output S and C_{out} respectively. Fig.9 shows the output of the normal 16-bit carry look ahead adder for the given inputs and the respective outputs are generated. Fig.10 shows the output of the pipelined fast multiplier of 16-bit using the ISA adder for given inputs A and B and output C is generated. Fig.11 shows the output of the conventional 16-bit multiplier for the given inputs and outputs are generated.

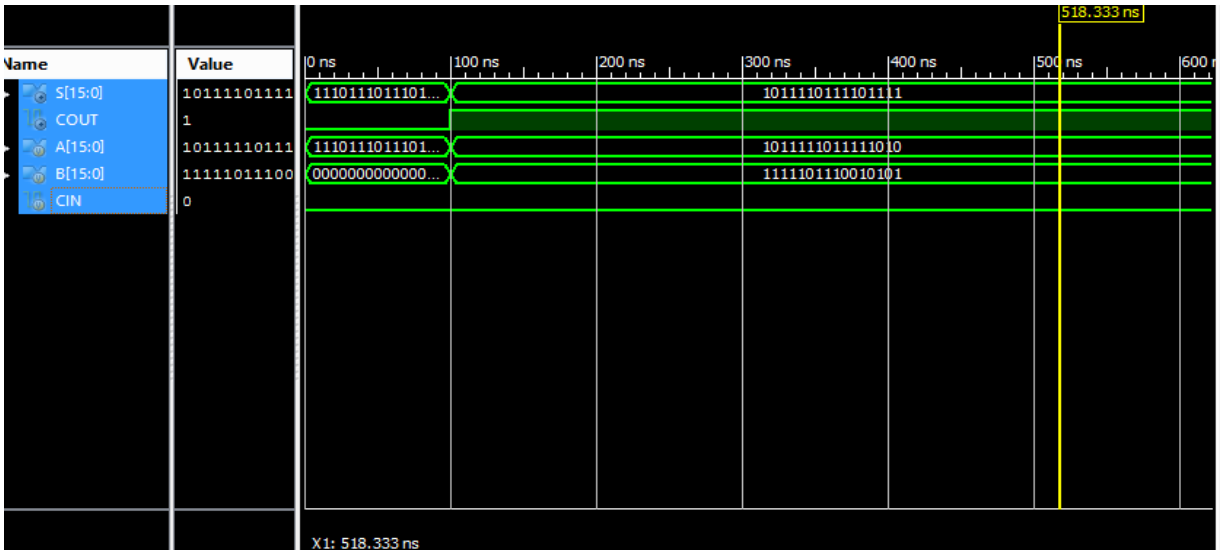

Fig. 8: Pipelined 16-bit ISA based CLA output

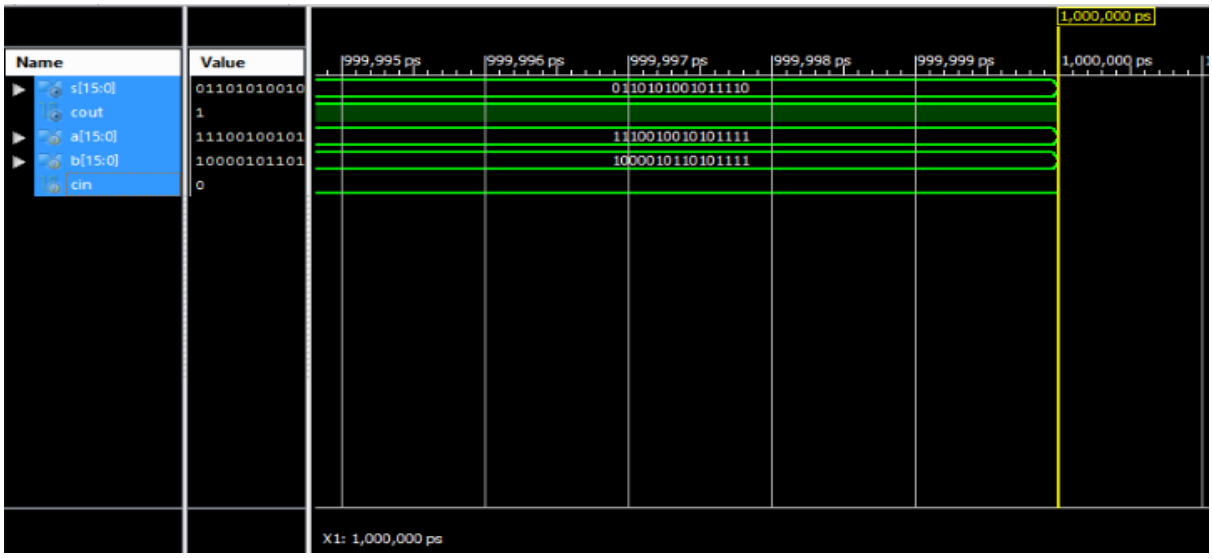

Fig. 9: Normal 16-bit carry look ahead adder output

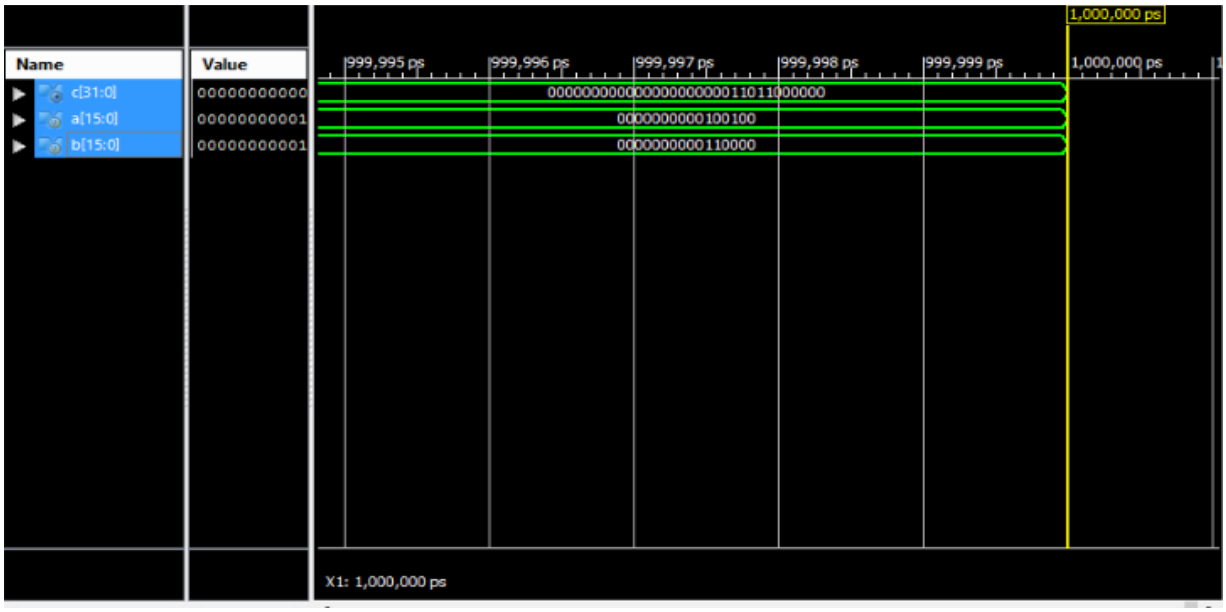

Fig. 10: Pipelined fast multiplier 16-bit using ISA adders output

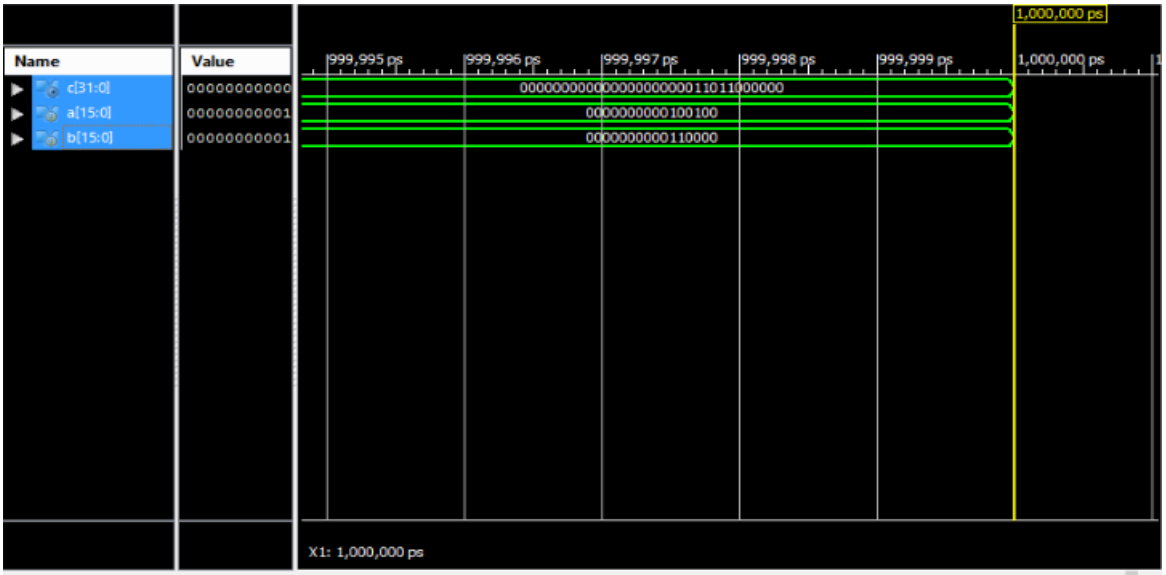

Fig. 11: Conventional 16-bit multiplier output

Table.1: Comparison table for Normal carry look ahead adder with pipelined ISA adder

Adder	Logical delay (ns)	Routing delay (ns)	Total Delay (ns)
Normal	15.754	8.932	24.686
Pipelined ISA	8.749	4.020	12.769

Table.2: Comparison table for Normal multiplier with pipelined ISA multiplier

Multiplier	Logical delay (ns)	Routing delay (ns)	Total Delay (ns)
Normal	57.722	39.354	91.076
Pipelined ISA	27.722	19.354	47.076

5. Conclusion

In this paper the detailed study and design and comparative analysis inexact speculative adders and multiplier was implemented for the reduced delay and high speed. From the above observations we can conclude that using of the inexact speculative adder based CLA improves the speed of execution over the normal carry look ahead adder and reduced the delay up to 48.27% and coming to the pipelined fast multiplier using the ISA adder improves the speed of execution when compared to normal multiplier and reduces the delay up to48.32%. We can also use the inexact speculative adders in many applications such as in multipliers, arithmetic and logic units and also used in the filters of the digital design.

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