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Research Paper

An improved 1-φ rectifier system using fuzzy logic control with 3-φ variable frequency drive

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Abstract

A 3-Φ VFD is fed from a 1-Φ AC supply. To stop more stresses in the components within the drive and within the input supply, the drive output power should be restricted. To beat this problem, several VFD makers decided that drive to be de-rated. As often as possible, the drive's output frequency is limited, supported the dc voltage ripple hence the DC capacitors aren't overstressed. Although, the traditional technique reduces the stress of the DC capacitor, it doesn't consider the stresses in other parts of the drive, particularly the diodes at the input and terminal blocks of input. This paper presents a new method to protect the drive using the Q-axis current with FLC. The motor's q-axis current shows information about the stress of each part of the VFD includes an input diode, an input terminal block and a DC bus capacitor. We recommend limiting the output power by reducing the output frequency based on the average amplitude and ripple of the current of the q-axis instead of the DC-bus voltage ripple. To demonstrate this concept, the traditional DC bus ripple voltage based method is compared to the proposed method using a low-power VFD powered by a single-phase AC power supply.

Keywords: *AC to DC converter; Dc ripple method; Fuzzy logic controller (FLC); VFD.*

1. Introduction

In most of the rustic areas, owing to the omission of 3-Φ AC supply, 3-Φ VFDs are implemented to work from a 1-Φ AC power. When using a 1-Φ ac power, the input current flowing into the 3-Φ VFD is three times (or at least double) the current flowing into the 3-Φ VFD when using the 3-Φ Ac supply. There are bound problems that are to be addressed on the victimization of 3-Φ drives with 1-Φ supply. The primary concern is a warming of capacitors owing to higher current ripples and the secondary concern is prodigious the peak values of current of input side diodes. Sadly, for few systems, diodes peak current rating might be lesser the dc current ripple capability of the Dc electrical condenser. For some systems, the drives o/p power is restricted by victimization of solely the DC ripple voltage based frequency fold-back methodology. Due to this technique, stresses occur in the diode rectifiers. This can scale back the reliability of the diodes. Correspondingly, some needs to be anxious with a continuous current rating of the input side diodes and also the terminal blocks of input. For several systems, diodes are having the capability to maintain the upper values of Root Mean Square current. However, the terminal blocks aren't having the capability to maintain the higher currents on a continuing basis. To beat this concerns, several VFD makers 3 broad ways that of handling 3-Φ VFD's high powered from a 1-Φ Ac supply. They are a) de-rating of VFD's, b) Usage of external hardware [1], c) using of management algorithm to attenuate the stresses within the VFD [2].

The traditional 1-Φ boost converter technique is shown in figure 1 used for feeding a 3-Φ VFD from 1-Φ ac power. A 1-Φ full bridge rectifier is used for converting ac to dc from that boost inductor is used for charging and discharging of energy. The main drawback of this technique is, switch T1 carries higher peak current and has higher voltage stress. Ripple across Dc is more than it is hard to remove the second harmonic ripple without pointedly increasing the dc capacitor size.

The operating principle of the front end rectifier system and mode of operation is shown in figure2 [1].a particular time instant, the bidirectional switch is kept for charging and discharging the passive elements. It is a 1-Φ partial boosting device. The main demerit of this topology is the boost electrical device is giant in size. Therefore, bidirectional switch is charged two times for each 50Hz cycle. Hence, the switching frequency is double the supply frequency.

The proposed FLC topology permits the VFD to supply the rated power while not the requirement of derating. Bound management algorithmic rule techniques are used in conjunction with the de-rating possibility.

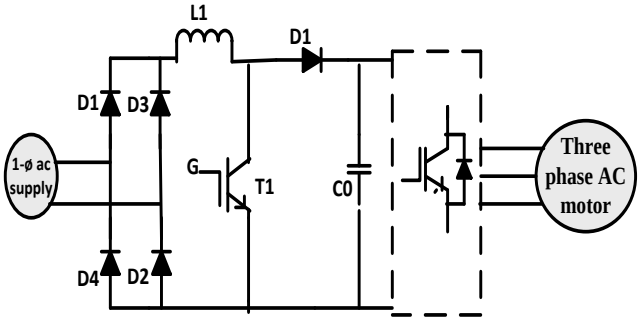

Fig.1 Conventional 1-Φ boost converter.

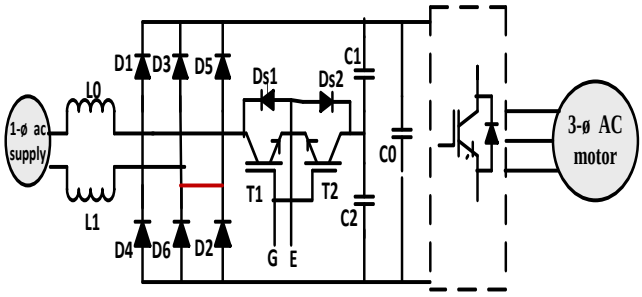

Fig.2 Improved 1-Φ active front-end rectifier circuit.

For the above-mentioned circuit, frequency fold-back is applied by using the Dc capacitor shown in fig2. Which is known as Dc voltage ripple based frequency fold-back technique. This technique mainly depends on the dc capacitor ripple voltage [2]. The dc capacitor current ripple is directly proportionate to the Dc capacitance ripple voltage. This ripple is measured therefore, the drive's o/p frequency is dropped. Consequently, the output power is limited and within a method, the current ripple over the capacitor is limited. Controlling technique is shown in fig 3.

This conventional technique has PI control algorithm. The dc voltage is measured. By using that we know the ripple voltage (which is obtained from high and low values of the voltage across Dc). If those measured dc voltage is more than those activation level, which tunes the foldback function this decreases the frequency and also the output power.

But this technique may decreases the o/p frequency and so the o/p power is limited, it is still more than what diodes at input can handle on a continual basis. This technique doesn't reduce the highest currents passing in the diodes, as well as in the terminal blocks. In this conventional method, thermal stresses are still existed due to level shifting from 1-Φ to 3-Φ.

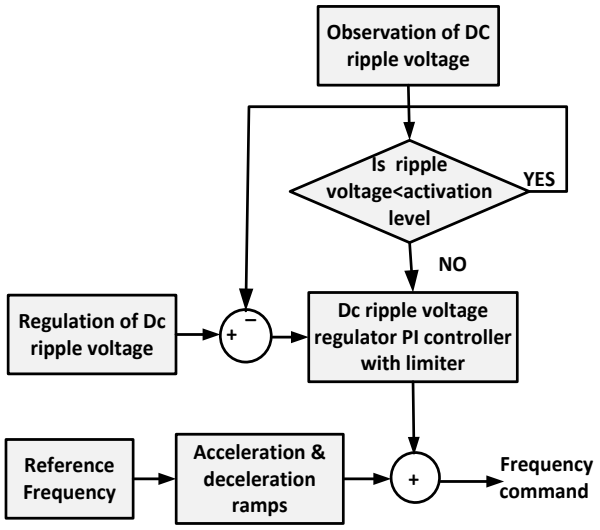

Fig.3 Controlling for DC voltage ripple based frequency fold-back technique.

2. Proposed technique

In the planned technique (Iq current based frequency fold-back technique with fuzzy logic controller) sponsors the utilization of a variable which is having knowledge about half stresses and is measured straightly instead of calculable. This method has knowledge of stresses on VFD and output load condition that shows an active current of the motor at that time 3-Φ VFD is fed from a 1-Φ power.

Due to certain drawbacks in the conventional methods, the proposed technique is applied on the motor side shown in figure 4. In this technique the motor is converted from a-b-c to d-q axis. In the d-q axis, d axis component is used for controlling of flux, and Q-axis component is used for controlling the motor speed then frequency also varies. Q-axis component having both fundamental and ripple I. e, 1. $I_{Q(avg)}$ Component, 2. $I_{Q(ripple)}$ Component. The $I_{Q(avg)}$ current is utilized to maintain the drive's output power. This may reduce the thermal stress inside the terminal blocks as well as stresses on the diodes at input and input terminal blocks. Peak-peak $I_{Q(ripple)}$ value is utilized to reduce the current ripple through the Dc capacitors, when low power VFD's are used. The twin bifurcate approach supports in ameliorate a VFD rating to be used with 1-Φ ac power. The voltage across dc is affected, when the I_q current having inconsistency by the outside factors, moreover as deterioration of the Dc Capacitance. If the minimization in average V_O because of deterioration of capacitors or because of delicate supply system or because of unbalanced voltages and in case extra burden applied at shaft of the motor these things reflects $I_{Q(avg)}$ current. Based on the size of the dc capacitor, Iq (ripple) current varies. Depending upon the load on the VFD steam at each driving point, the Iq average and Iq ripple are also affectd. This grant the frequency fold-back function to react the improvement in current ripple. Therefore, optimal values are achieved. The controlling technique for the proposed method is shown in figure 4. The technique have PI controllers. The primary controller regulates the utmost o/p quadrature axis avg current ($I_{Q(average)}$) that depends on size of the drive and its rated voltage.

The secondary controller regulates the quadrature axis current ripple ($I_{Q(ripple)}$ abundancy. Both controllers works severally but the quadrature axis avg current controller have more priority over quadrature axis ripple current regulator which depends on the relative peak current rating of diodes and the current ripple capability of Dc capacitors either the quadrature axis avg current controller or the quadrature axis current ripple controller is activated.

2.1. Quadrature axis average (Iq average) current based fold-back methodology.

In $I_{Q(avg)}$ regulator, the drive output $I_{Q(avg)}$ will be compared with those activation level. In those measured Iq value is more than those activation level afterword those PI of the average current controller is triggered. Those yield of the PI may be -ve and minimizes it from the reference frequency to produce a less frequency command. Whether the o/p quadrature axis current may be efficiently reaches the regulation level. This PI regulator bit by bit saturates to the less o/p frequency. Operation of quadrature axis avg current regulator with PI is same as in [2].

2.2. Quadrature axis ripple (I_q ripple) current based fold-back methodology.

In $I_{Q(ripple)}$ regulator, the steam output Iq ripple will be compared with those activation level. In those measured Iq value is more than those activation level after those PI of the ripple current controller is triggered. Those yield of the PI is negative and subtracts from the reference frequency to produce a less frequency. When ripple current regulator is triggered, it could make deactivated just if quadrature axis ripple current achieves under the deactivation level. This confirms the yield of the PI controller is operated only within those activation and deactivation stages thus preventing high o/p frequency such that the Iq(ripple) current reaches down to the regulation level. Those yield of the PI controller may be negative and further more subtracts from output frequency swings that might bring about information about high diode i/p current and capacitor high current. Operation of quadrature axis ripple current regulator with PI will same as in [2].

The better or optimal performance is achieved by using both avg

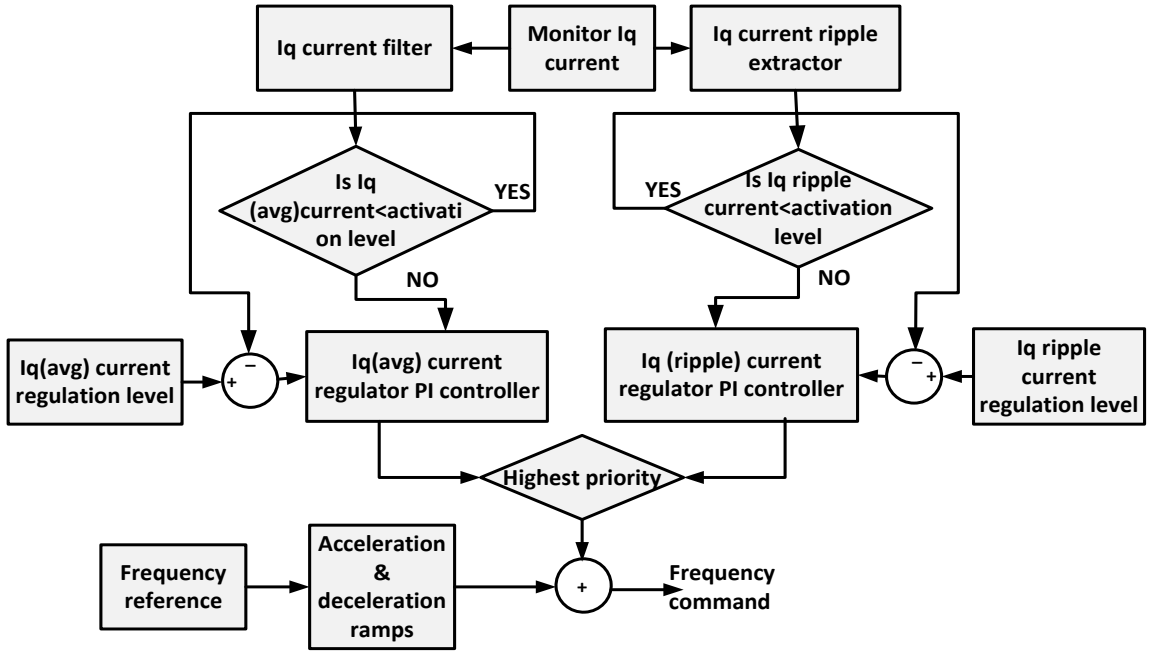

Fig.4 Controlling for the proposed technique

current controller and ripple current controller even when the supply is unbalanced or 1-Φ supply. The stresses are reduced due to the reduction in torque which maintains the power constant. If the torque is reduced, stresses on the drive also reduced. Here FLC is used in place of PI controller (shown in figure9) where the pulse is generated for bi-directional switch.

3. Fuzzy Logic Controller

Fuzzy logic depends on fuzzy set theory, in which a variable is a member of one or more sets, with a specified degree of membership. Fuzzy logic allows us to match the human reasoning process in computers, sanctify imprecise information, and make a decision based on unclear and unfinished data, although employing a "De-Fuzzification" process**.**

The FLC mainly consists of three blocks

i. Fuzzification.
ii. Inference mechanism.
iii. De-Fuzzification.

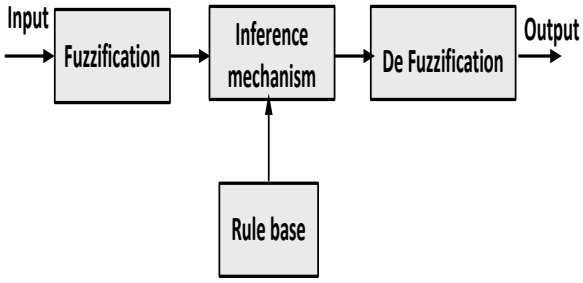

Fig.5 Block diagram of FLC**.**

Rules:

IF e is NB and de is NB then output is NB.

IF e is NS and de is NB then output is NB.

IF e is Z and de is NB then output is NS.

Like that there are 25 rules are formed. Triangular membership function is used.

4. MATLAB simulation results

In the proposed method a 7.6hp motor is used, 220volts, 1-Φ supply is powered by 3-Φ VFD.

4.1 Comparison of Fuzzy controller based method with conventional methods

The fuzzy controlled based method is compared with the two conventional techniques. In DC bus ripple voltage based fold-back technique, from 0-2 sec the applied mechanical torque to the induction motor is zero. After 2 sec we applied step torque (which is shown in figure 7) hence the ripple of the DC bus voltage increases and input current also increases. Thus triggers fold-back function to reduce the output frequency of the drive thus reduces the output power of the drive. Hence, at the end of 2sec dc bus ripple value is stabilized and reaches specified value. However, at the end of 3 sec the higher peak input currents flows in the circuit is shown in figure 10. In q-axis current based fold-back method with PI controller, from 0-2 sec the applied mechanical torque to the induction motor is zero. After 2 sec we applied step torque (shown in figure 7) hence the ripple of the DC bus voltage increases and Q-axis ripple current also increases. Thus triggers Q-axis ripple current fold-back function to reduce the output frequency of the drive thus reduces the output power of the drive. Hence from the end of 2sec dc bus ripple value and input current is stabilized and reaches its specified value is shown in figure 11. In q-axis current based fold-back method with FLC from 0-2 sec the applied mechanical torque to the induction motor is zero. After 2 sec we applied step torque hence the ripple of the DC bus voltage increases and Q-axis ripple current also increases. Thus triggers Q-axis ripple current fold-back function with FLC to reduce the output frequency of the drive thus reduces output power of the drive. Hence from the end of 2sec dc bus ripple

value and input current is stabilized and reaches its specified value is shown in figure 12.

TABLE 1: Tabular column for rules of FLC

e / *de*	NB	NS	Z	PS	PB
NB	NB	NB	NS	NS	Z
NS	NB	NS	NS	Z	PS
Z	NS	NS	Z	PS	PS
PS	NS	Z	PS	PS	NB
PB	Z	PS	PS	PB	PB

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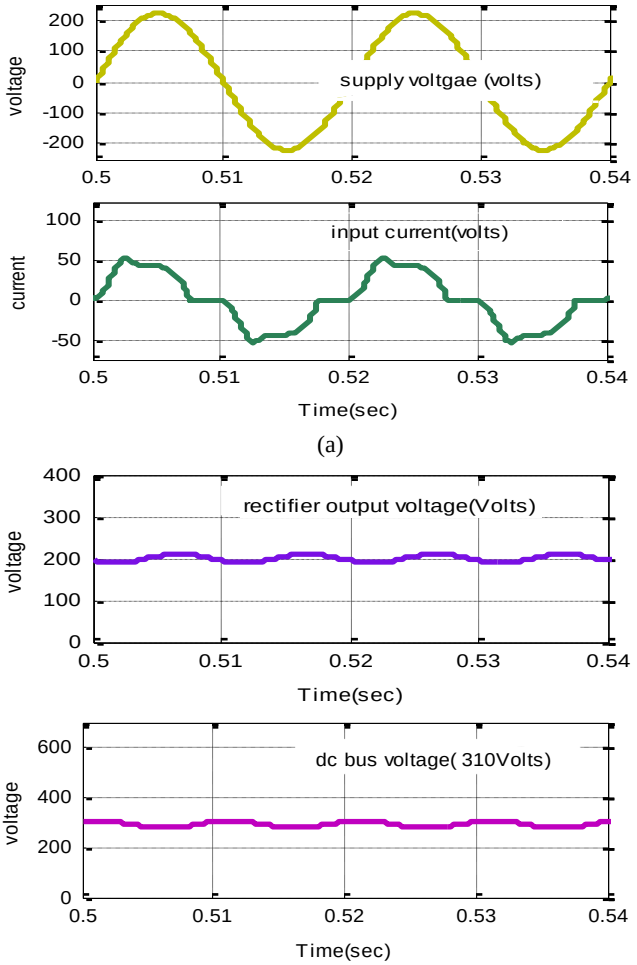


Fig.6 (a) supply voltage and RMS current (b) rectifier output voltage and dc bus voltage.

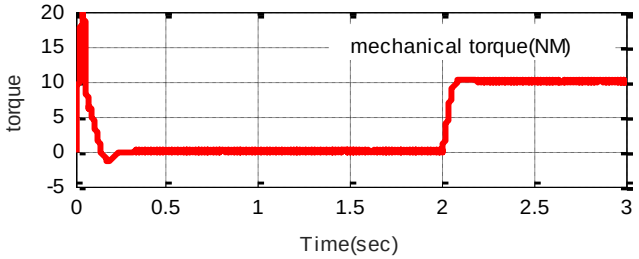


Fig.7. mechanical torque (NM)

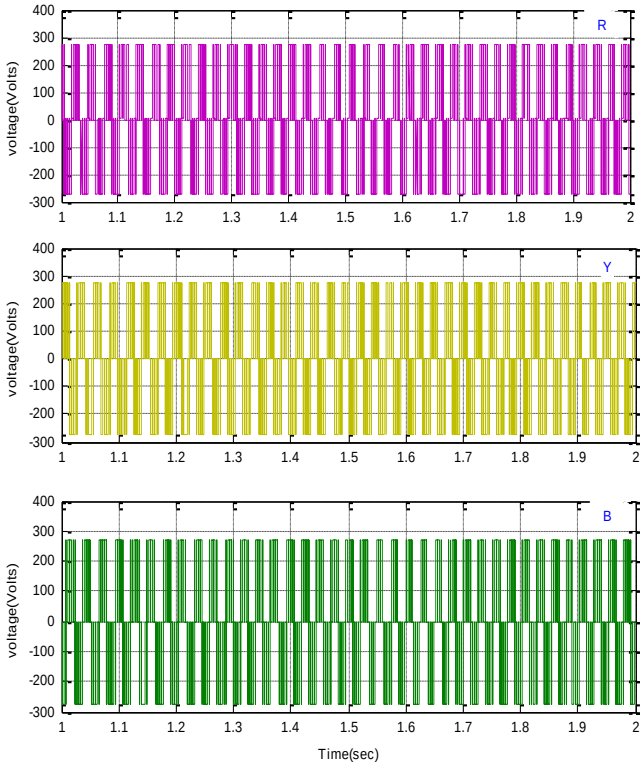
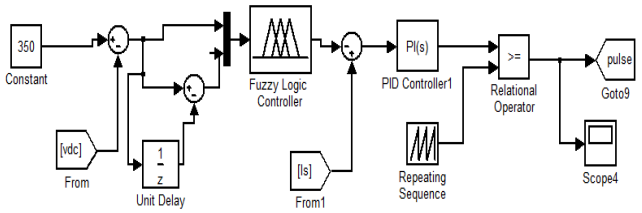


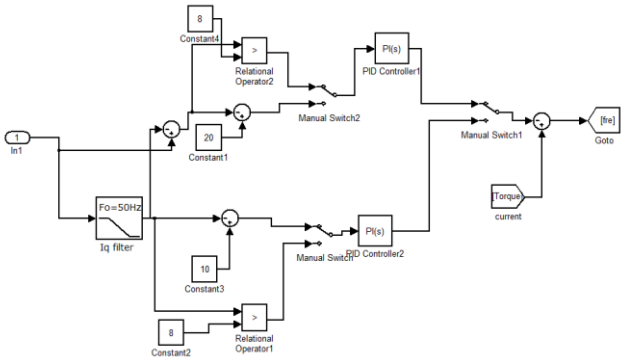
Fig.8 inverter output voltage (line-line).

TABLE 2: specification for the 1-φ vfd application.

	$230V_{ac}$
No of phases	One
Rated Motor power	7.6hp
rated voltage and motor phases	3-Φ,220Volts
L0=L1	1.163mH
C1=C2	258.54UF



(a)



(b)

Fig.9 MATLAB Simulink diagram for(a) generation of pulse for bidirectional switch.(b) Q-axis current based frequency fold-back method with FLC.

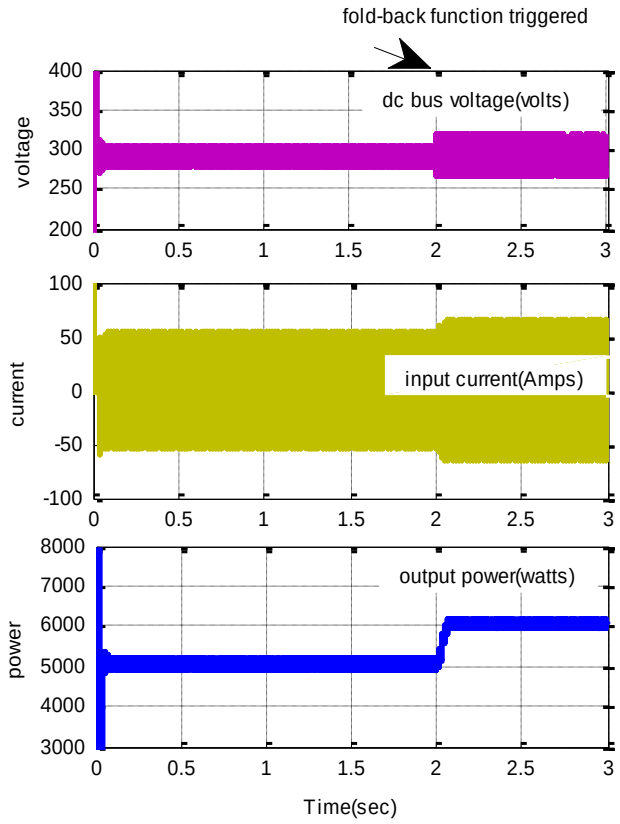


Fig.10 dc bus voltage ripple based frequency fold-back method.

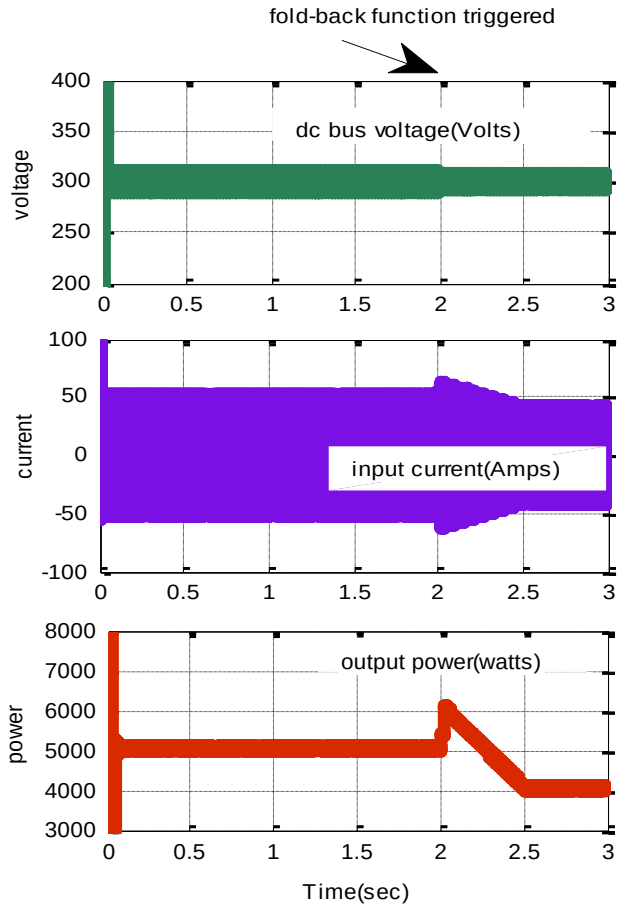


Fig.11 Q-axis current based frequency fold-back method with PI controller.

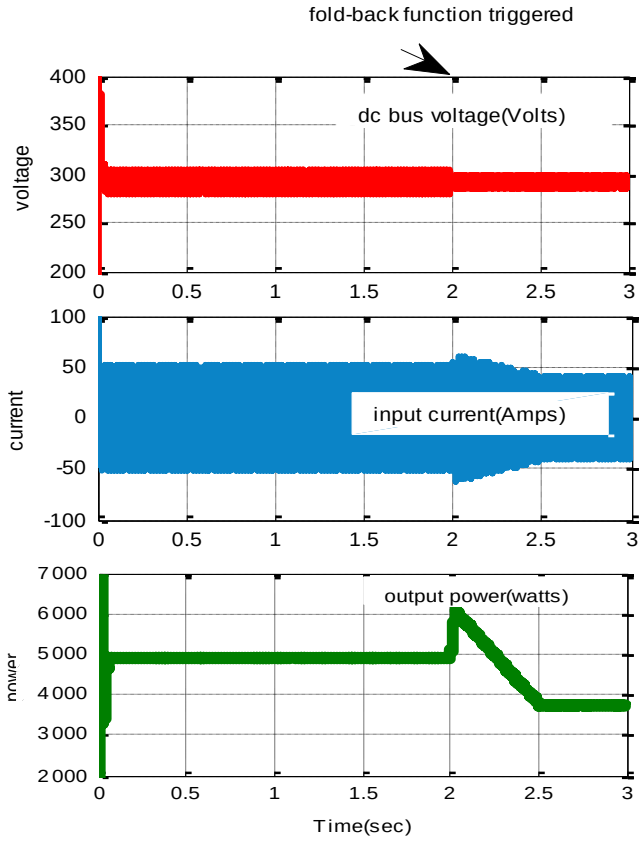


Fig.12 Q-axis current based frequency fold-back method with FLC controller.

TABLE 3: Simulation results for three methods.

Steady state values	Peak to peak dc voltage	Peak to peak input current	Output power	Input current THD
Dc bus ripple voltage	40V	60A	7.6hp	26.16%
Q-axis current with PI controller	20V	45A	5.36hp	25.89%
Q-axis current with FLC.	12V	40A	2.68hp	25.21%

5. Conclusions

As shown in the comparison of the conventional method and the q-axis method with fuzzy controller technique for a 3-Φ VFD is operating from a 1-Φ AC power. The given below conclusions are made

1. The major thought is based on storing energy in an external inductor and retrieving it at the appropriate time to transfer it to the load in an efficient and optimal manner.
2. The most important disadvantage of the DC bus voltage ripple fold-back method is that it does not consider component stresses in other parts of the VFD, such as input diodes and terminals, rather than DC bus capacitors.
3. For better performance quadrature axis based frequency fold-back method with FLC is used. In this technique both the voltage ripple, peak to peak currents are regulated.

4. The quadrature axis ripple current is used to limit the dc capacitor ripple and the diode peak current, although quadrature axis avg current is used to limit the drive's RMS current through terminal blocks and o/p power.

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