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Research Paper

Finite element analysis of heat sink in term of thermal and temperature distribution with different chip power input

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Abstract

This paper presents the simulation of heat sink by using Workbench 18.0 Software to simulate the temperature distribution at different chip power input. 3D model of heat sink is generated using Design Modeler using the same dimension with experimental setup. The study was made for a heat sink mounted on the power source (Chip) under different types of chip powers. The results are presented in terms of temperature distribution when chip powers have been increased from 1 W to 10 W. The temperature distribution is been observed and it was found that the temperature distribution of the heat sink has lower temperature when power source at 1 W and increase significantly when the power source rise up to 10 W. The increase the temperature of heat sink is from 30.8ºC up to 96.2ºC estimated to be 212% the increase of temperature. The simulation also been verify by using different time step use during the simulation and using grid independency test to ensure the simulation result is accurate.

Keywords: *Chip power; Finite Element analysis; Heat sink; Temperature distribution.*

1. Introduction

Advances in the field of electronics have resulted in significant increase in power input, high performance and emerging trend of miniaturization of modern electronics [1-3]. This resulted in dissipation of high heat flux at chip level, heat sink and other electronic components. In order to improve the performance and reliability of heat sink, improvements in cooling technologies are required [4-6]. As a result, thermal management is becoming important and increasingly critical to the electronics industry [7-10]. The task of maintaining acceptable junction temperature by dissipating the heat from integrated circuit chips and heat sink is significant challenge to thermal engineers [11]. However, the physical means associated with enhancing computing capabilities at the electronic component have also created a very challenging set of circumstances for keeping electronic devices cool, a critical factor in determining their speed, efficiency and reliability [12]. Natural convection cooling is obviously advantageous for low power dissipating of heat sink since it offers a low-cost, energy-free and noise-free operation [13]. Numerical analysis is used to model natural convection cooling of heat sinks using electronics cooling software. The analysis evolves in two stages: a numerical simulation of the detailed heat sink and a simulation of a compact model that exhibits similar thermal and flow resistance characteristics to those of the actual heat sink[14]. The development of a computationally efficient computer-aided design (CAD) method which uses a finite element numerical model (FEM) coupled with empirical correlations, to create an optimum heat sink design, subject to multiple constraints. A thermal optimization of heat sink design specification includes constraints upon size, total mass and air coolant pressure drop across the heat sink [15].

Air-cooling characteristics of an electronic devices heat sink with various square modules array have been experimentally investigated. Aluminium block of module array was made and the base temperature of modules array of 40-100ºC were adapted to estimate the average heat transfer coefficient between the flowing air and modules array outer surfaces. The results indicated that the average heat transfer coefficient little increased with increasing the modules array temperature, but the increase was significantly higher with increasing the flowing air velocities [16].

2. Methodology

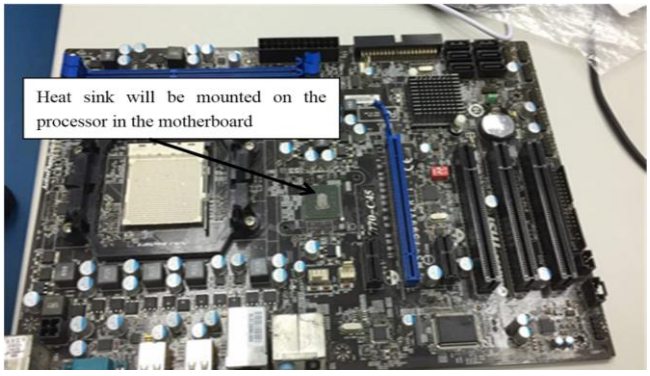


Fig. 1: Simulation setup for heat sink mounted on the motherboard (top view).

Table 1: Dimension of components used in simulation.

Component	Quantity	Size (cm)
AC/ DC power supply	1	1-10 Watt
Motherboard	1	33.3 cm × 0.15 cm × 8 cm
Chip	1	2 cm × 0.3 cm × 2 cm
Heat sink	1	2 cm × 0.1 cm × 2 cm

3. Results and discussion

The simulation of heat sink by using Workbench 18.0 software to simulate the temperature distribution at different chip power input. 3D model of heat sink is generated using Design Modeler using the same dimension with experimental setup. The study was made for a heat sink mounted on the power source (chip) under different types of chip powers. The results are presented in terms of temperature distribution when chip powers have been increased from 1 W to 10 W. The temperature distribution is been observed and it was found that the temperature distribution of the heat sink has lower temperature when power source at 1 W and increase significantly when the power source rise up to 10 W. The increase the temperature of heat sink is from 30.8ºC up to 96.2ºC estimated to be 212% the increase of temperature. Figure 1 shows the temperature distribution of heat sink using chip power 1 Watt to10 Watt. Meanwhile, Figure 3 shows the graph plot of temperature distribution of heat sink at different chip power.

In order to get the precise result in simulation, the validation of CFD simulation based on time step, no. of times step and max no. iteration must be made. There are a few no. of times steps use for example 10, 20, 30 and 100 with constant time step. At the same time, number of max iteration also been used differently (10, 20, 30 and 45) to ensure the result already consistent and converge. Figure 4 shows the graph plot of temperature distribution of heat sink at number of times step and max number of iteration.

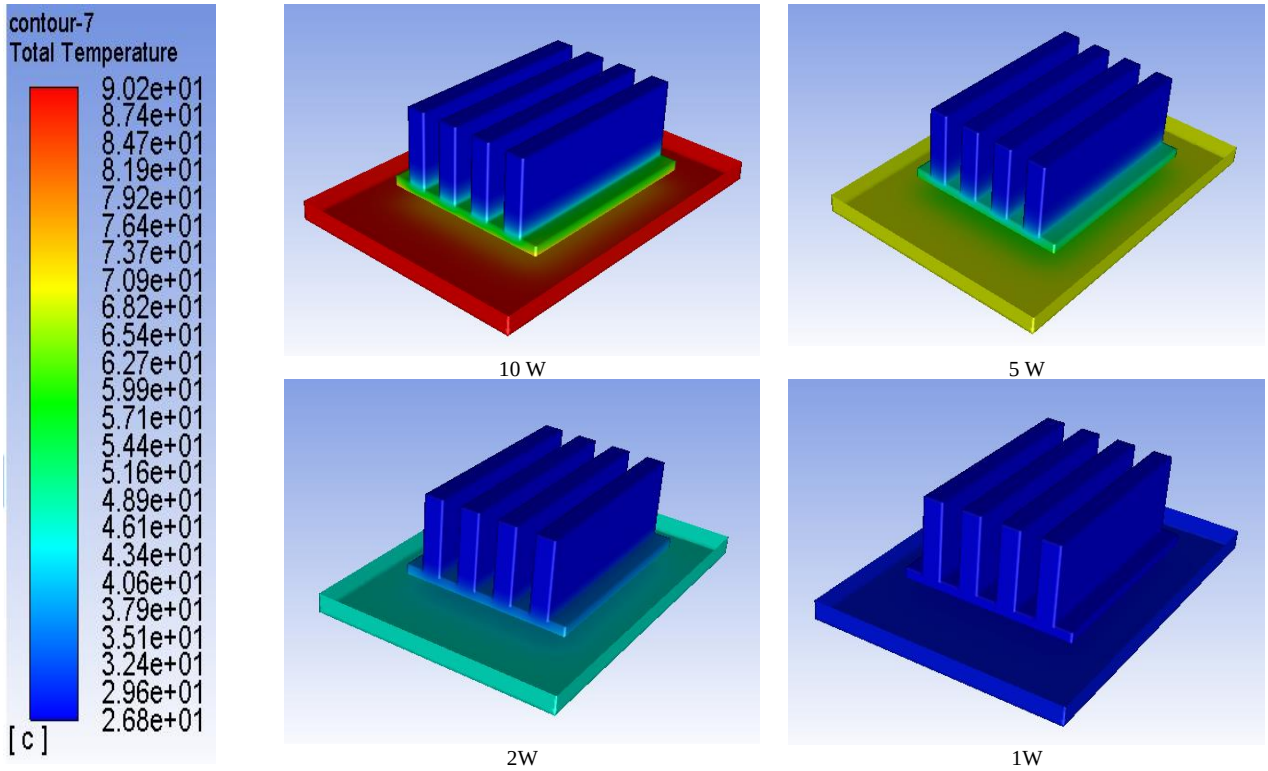
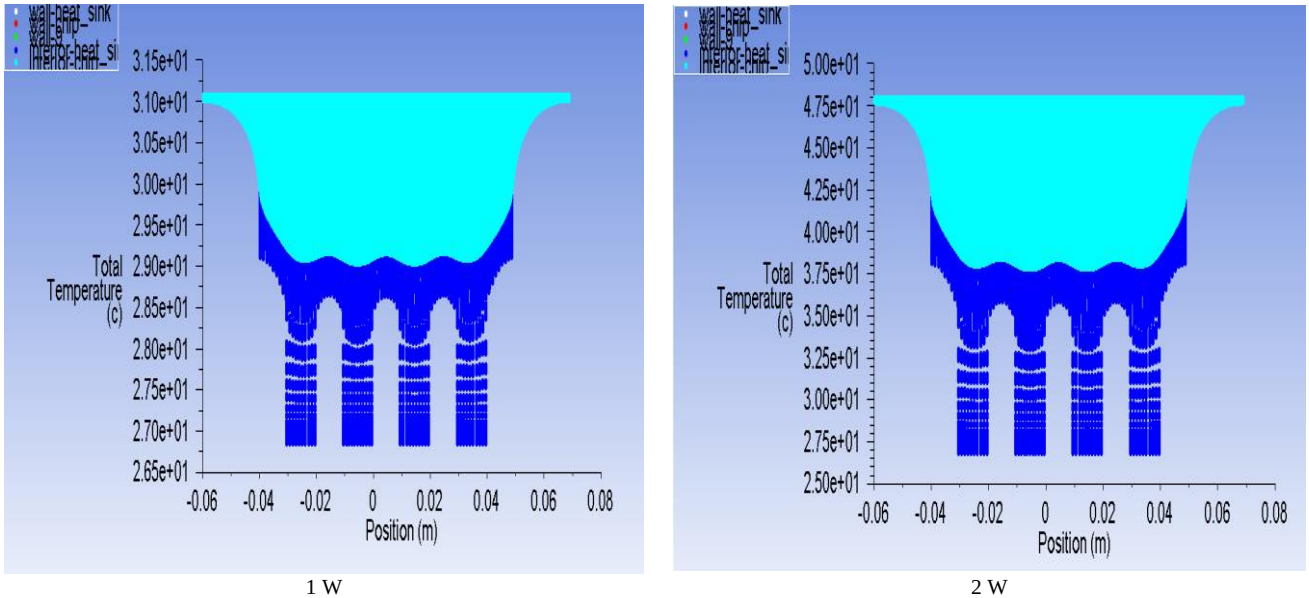
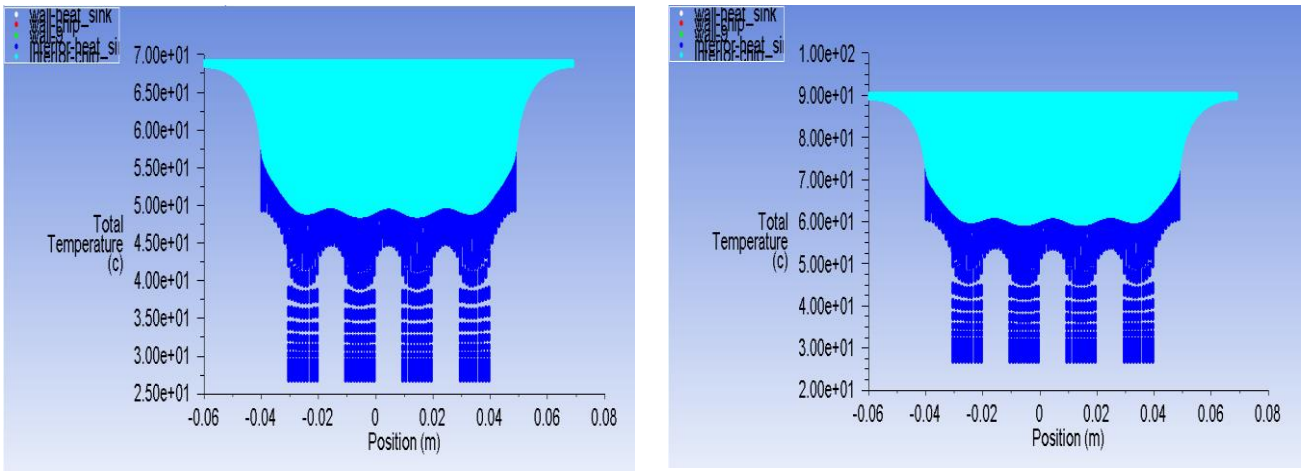


Fig. 2: Temperature distribution of heat sink using chip power 1 W to10 W.

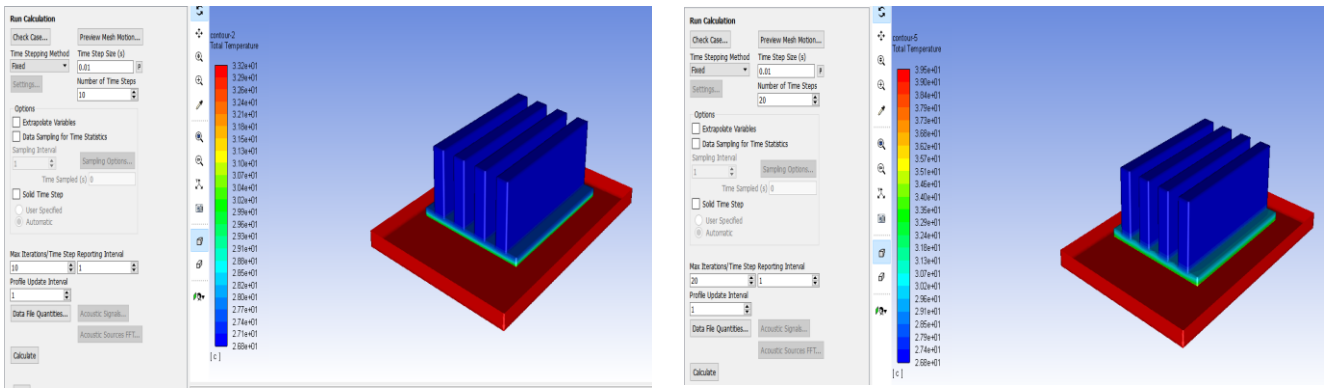


1 W 2 W



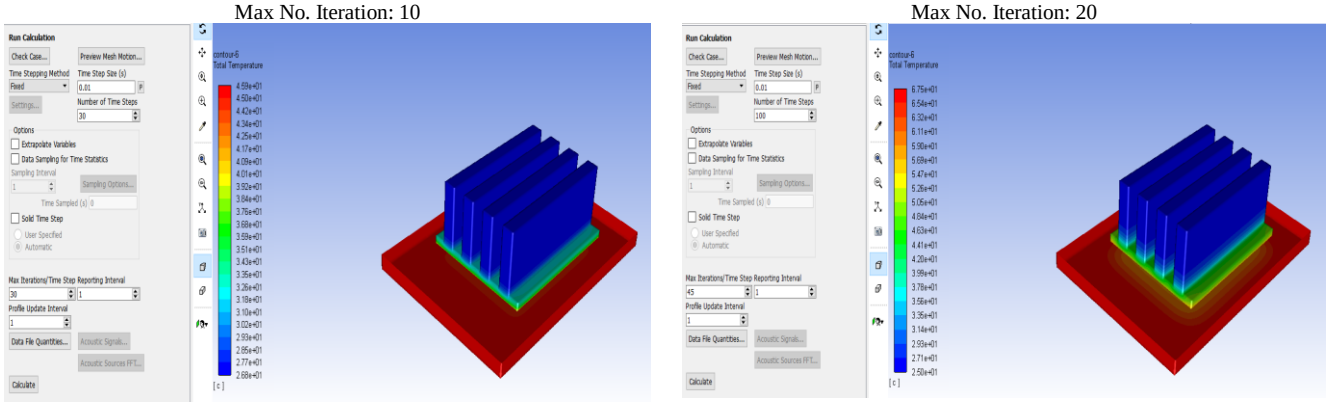
5 W 10 W

Fig. 3: Graph plot of temperature distribution of heat sink at different chip power.



Time step: 0.01
No. of Times Steps: 10
Max No. Iteration: 10

Time step: 0.01
No. of Times Steps: 20
Max No. Iteration: 20



Time step: 0.01
No. of Times Steps: 30
Max No. Iteration: 30

Time step: 0.01
No. of Times Steps: 100
Max No. Iteration: 45

Fig. 4: Graph plot of temperature distribution of heat sink at number of times step and max number of iteration.

4. Conclusion

From the results above, it can be concluded that the temperature distribution of heat increase with increase of chip power from 1 W to 10 W. The maximum percentage of temperature distribution of heat sink at 10 Watt with 1 Watt is 212% and the maximum temperature for the heat sink is 96.2ºC at chip power 10 W. At the same time, the number of times step and max number iteration also give great significant to the temperature distribution to the heat sink. The temperature at low no. of times step are not accurate and the temperature still rising because it not converge yet. The temperature can only be taken when the iteration is converge.

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