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Research Paper

Level Converters for Ultra Low Power IoT Applications

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Abstract

For efficient ultra-low power IoT applications, working with various communication devices and sensors which operating voltages from subthreshold to superthreshold levels which requires wide variety of robust level converters for signal interfacing with low power dissipation. This paper proposes two topologies of level converter circuits that offer dramatic improvement in power and performance when compared to the existing level converters that shift signals from sub to super threshold levels for IoT applications. At 250 mV, the first proposed circuit - a modification of a tradition al current mirror level converter - offers the best energy efficiency with approximately seven times less energy consumption per operation than the existing design, but suffers from a slight reduction in performance. However, a second proposed circuit - based on a two-stage level converter - at the same voltage enhances performance by several orders of magnitude while still maintaining a modest improvement in energy efficiency. The Energy Delay Products (EDP) of the two proposed designs are equivalent and are approximately four times better than the best existing design. Consequently, the two circuit options either optimizes power or performance with improved overall EDP.

Keywords: *IoT, Level shifters, ultra-low power, subthreshold.*

1. Introduction

Internet of things (IoT) is an emerging technology whose building blocks of IoT are device layer (sensing end node), connectivity layer, central data processing and analytics (CDPA) layer and Application and management layer. IoT devices deal with sensing in order to extract the available information and communicating this information to users remotely at different locations. IOT devices are remotely located and operated in an energy constraint environment. The number of devices connected increases exponentially so it becomes a challenging issue to provide power based on the application setup.

Different circuit components in a SOC need different power supply based on its performance and power requirements. Normally, sensor based end nodes are battery based which have limited lifetime, require regular replacement and are very bulky. In IoT devices which require standalone independent operation with less maintenance such attributes are undesired. To save and optimize power requirement and to extend the lifetime of the IoT devices, many techniques are used such as Energy harvesting, transiently powered system and many other low power techniques. Many IoT devices operate on Low power bases. All the above methods use Voltage converters in some stage of their design. [1-2]

The present day IoT (Internet of Things) Technology demands the interaction of the wide variety of sensors, interconnects and very high speed performance with low power and various operating voltage ranges from sub threshold to super threshold levels. Subthreshold logic gives us the lowest energy per operation when compared to circuits that operate at traditional supply voltages [3-5]. However, running at this non-standard very low voltage operating point limits performance, which may not be acceptable for medium to very high performance applications (e.g. wireless micro-sensor networks, bio-sensors and warfare electronics, etc.)But the major challenge is that thesecircuits become less robust and more prone to environmental and manufacturing factors which leads to degradation in the performance.Temperature and across-chip may affect the transistor threshold voltage and which leads to an exponential effect on the drive capability of the transistor.So there is demand for the Circuits which consume less power and better performance.

Traditionally, level converters were employed exclusively to allow chip internal signals to be transmitted to the outside world through the pad ring, which often operated at a different voltage in order to maintain compatibility with older technology used at the system level. More recently, with the increased use of voltage islands within chips, functional units are being operated at different voltages to allow for performance critical circuits to operate at higher voltages while simultaneously allowing all other non-critical circuits to operate at a lower voltage to improve the energy efficiency.

[6] Reported that optimized multi-V_{dd} with multi-V_T designs provide a dramatic dynamic power reduction by 40-50% as compared to the traditional single V_{dd} designs without compromising performance. In order to effectively interface critical cells at higher voltages with non-critical cells at lower voltages, level converters are required to completely turn *off*the PFET transistor which requires the gate node to be driven to a voltage exceeding the lower supply voltage. The difference in

voltage – if more than the threshold voltage of the transistor – can result in the PFET permanently remaining active. Level converters eliminate this voltage difference to allow for proper CMOS operation.

This paper presents an evaluation of a wide range of level converters in the context of converting signals from subthreshold to superthreshold levels. Two proposed level converters described provide a significant improvement in the Energy Delay Product (EDP) relative to the existing level converters while interfacing these disparate voltage levels.

2. Existing Level Converters

Conventional level converter circuits include the half-latch and the current mirror designs as shown in Fig. 1 (a) and (b) respectively. The Traditional Half-Latch (THL) level converter circuit has the advantage of a simple design and is well suited for higher core voltages. However, for low input supply voltages, the performance degrades as the NMOS devices (operating essentially with leakage in subthreshold regime) are incapable of overcoming the drive strength of the super-threshold PMOS half-latch.[9]

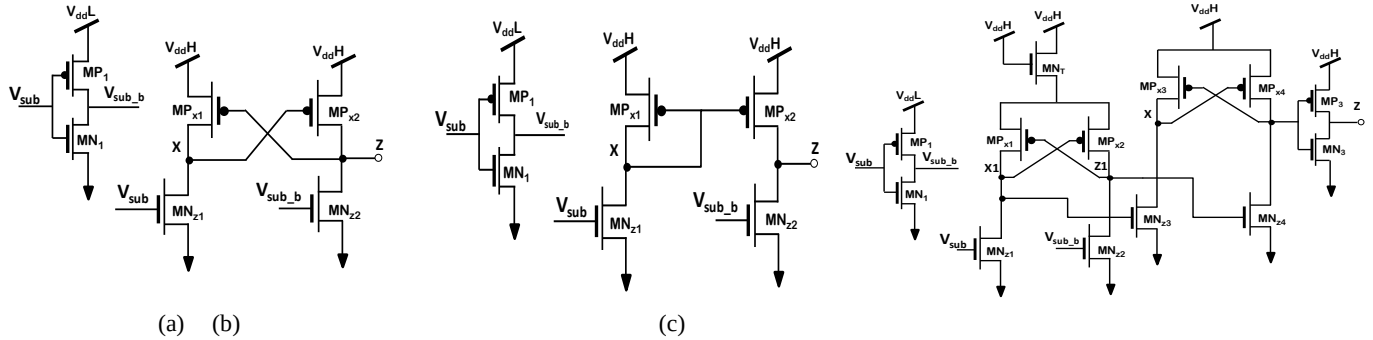
In fact, for typical transistor sizings, this circuit does not operate at all when converting subthreshold signals. However, the latch will function correctly if the NMOS transistors, MN_{z1} and MN_{z2}, are sized substantially larger than the PMOS transistors, MP_{x1} and MP_{x2}, in terms of widths. On the other hand, the Traditional Current Mirror (TCM) level converter design, as shown in Fig. 1(b), provides improved performance and stable current driving capability compared to the half-latch design by replacing the PMOS half-latch with a PMOS constant current mirror load. The TCM design is well suited for a wide range of voltage conversion with regards to performance; however, the design suffers from increased power consumption resulting from the leakage path formed by either PMOS transistors, MP_{x1} or MP_{x2}, in the current mirror and one of the NMOS pull-down devices, MN_{z1} or MN_{z2}, which is always *on* in a static sense.

The third level converter [7] considered is based on a Traditional Two-Stage (TTS) version of the THL design as shown in Fig. 1(c). The first stage uses a half-latch that is powered by a degraded supply voltage with a threshold voltage drop from a NMOS diode. Therefore, the signal provided to the second stage half latch ranges between 0 and V_{dd}-V_t. The second stage is a conventional half-latch stage, which serves the purpose of restoring the output voltage to full swing. Although this design aptly alleviated many of the issues with converting subthreshold signals, [7] additionally required the combined use of the following circuit methods: 1) multi-threshold devices – implementing higher VT devices to reduce dynamic energy and leakage current for *off* devices, and lower VT devices for increased drive current necessary to overpower the PMOS transistors in the first stage; and 2) subthreshold device sizings – adjusting the width and length ratios of the devices at subthreshold to overcome the current imbalance. These techniques result in increased cost and processing complexity and were therefore not included in the evaluation of this converter design. Consequently, the TTS circuit did not perform as well as originally reported; however, two level converter circuits - inspired from the TTS - are proposed and evaluated in the following section, which not only provide energy efficient subthreshold operation but also enhanced performance as compared to TTS.

Many other level converter circuits have been reported but were not included in this analysis for a variety of reasons. [8] Used a combination of thick and thin gate oxides to provide robust operation from ultra low to high voltage ranges - increasing the cost of standard CMOS process. A similar restriction exists in [9] where improvements were gained in the performance of the THL and TCM by implementing Dynamic Threshold CMOS (DTCMOS). DTCMOS ties the gate and body of the input transistors and thus dynamically adjusts the threshold via the body effect. The connection is not normally possible in the superthreshold regime as the source to body junction would forward bias and result in significant leakage current. Although, subthreshold voltage levels eliminate this biasing problem, the restriction of only using subthreshold input levels eliminated this design from consideration. The level converters described in [10] were not considered as these included pass gate inputs, which are susceptible to above-V_{dd} and below-ground noise as well as being a potential source of reverse stage leakage at lower subthreshold range. Additionally, the design failed to operate at subthreshold levels.

Furthermore, for each of the traditional level converters described, an incremental improvement is possible by adding a voltage doubler at the input of the level shifter. Voltage doublers have been proposed in [11-12] that bootstrap the true and complement signal to almost double the voltage of the input signal. For subthreshold circuits, this means that the doubler output is typically raised to superthreshold levels (e.g. 250 mV doubled to 500 mV) and this increase has an exponential impact on the drive strengths of the NMOS devices used subsequently in the level conversion – significantly improving performance. Unfortunately, voltage doublers have two fatal flaws. First, the voltage doubler includes two large transistors used as MOS capacitors necessary for boot strapping the input voltage and this results in a prohibitive increase in circuit area. Second, bootstrapping circuits are generally not used in industrial designs as nodes are at times left floating and are therefore susceptible to noise and are difficult to test. The susceptibility to noise arises as a result of one of the two capacitor plates being mutually exclusively floated above the supply voltage. This floating capacitor can be discharged inadvertently by a variety of sources (i.e. Radiation, capacitive coupling, leakage, etc.). As a result, voltage doublers were eliminated from consideration in this analysis.

Finally, the level converter circuits based on Wilson current mirrors [13] failed to provide full swing operation at the output for any device sizings in the CMOS technology used in this analysis (45nm IBM). However, two proposed designs described in the next section, which are modified versions of this Wilson current mirror with an additional stage added, not only provided rail-to-rail operation but also excelled in performance when compared to all existing circuits with equivalent or better energy efficiency levels.



(a) (b) (c)

Fig.1. (a) Traditional Half-Latch based level converter (THL) **(b)** Traditional Current Mirror based level converter (TCM) and **(c)** Traditional Two-Stage level Converter (TTS)

3. Proposed Level Converters

As described previously for subthreshold level converters, the primary obstacle is the disparity in drive strengths between the pull-up PMOS transistors and pull-down NMOS transistors. Several solutions have been proposed, which essentially employ either weakening the drive strength of pull-up PMOS transistor or increasing the drive strength of the pull-down NMOS transistor. The first proposed solution in this study extends the concept of the conventional current mirror load by adding levels of cascode current mirrors to the TCM, as shown in Fig. 2(a) and (b), referred to as Proposed Cascoded Current Mirror (PCCM).

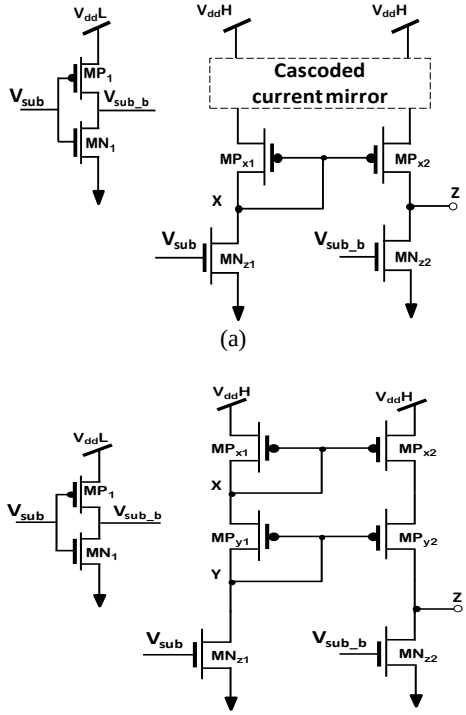


Fig. 2.(a) General form of the proposed cascode current mirror based level converter and **(b)** Specific example of thecurrent mirror based level converter, in which a single cascode current mirror circuit is added to the TCM circuit (PCCM1).

A family of new level converters is created that offer varying levels of trade-off between performance and power consumption. The levels of cascode current mirror circuit essentially act as a series of current limiters that reduce the drive strengths of the pull-up PMOS transistors. This simple technique was extended to include up to four cascode stages in addition to the basic TCM circuit. The stages were added such that the full output voltage swing remained possible. The biggest advantage of this technique is eliminating the necessity for large pull-down NMOS transistors. The resulting circuit permits operation over a wide input supply voltage range and additionally reduces static and dynamic power consumption by several orders of magnitude. Fig. 2(a) shows the generalized circuit while Fig. 2(b) illustrates a specific example where a single cascode current limiter stage is added to TCM.

As discussed in the previous section for reliable operation of the TTS circuit, [7] requires multi-threshold devices and subthreshold device sizings. In this study, a modified version of the TTS is proposed that provides enhanced performance and energy efficient operation without imposing the above mentioned design and fabrication constraints. The second and third proposed designs replace the first stage of the TTS design, i.e. the half-latch circuit, with either a Wilson or Modified Wilson current mirror. Additionally, similar to the original design, the first stage is powered with the degraded virtual supply from the NMOS diode. These two proposed designs preserve the second stage, half-latch circuit, to provide full swing voltage operation. The modified TTS circuits are; 1) a Proposed Two Stage with Wilson current mirror (PTSW), based on regular Wilson current mirror circuit and 2) a Proposed Two Stage with Modified Wilson current mirror (PTSM), as shown in Fig. 3(a) and (b) and their layouts are shown in 4(a) and 4(b) respectively.

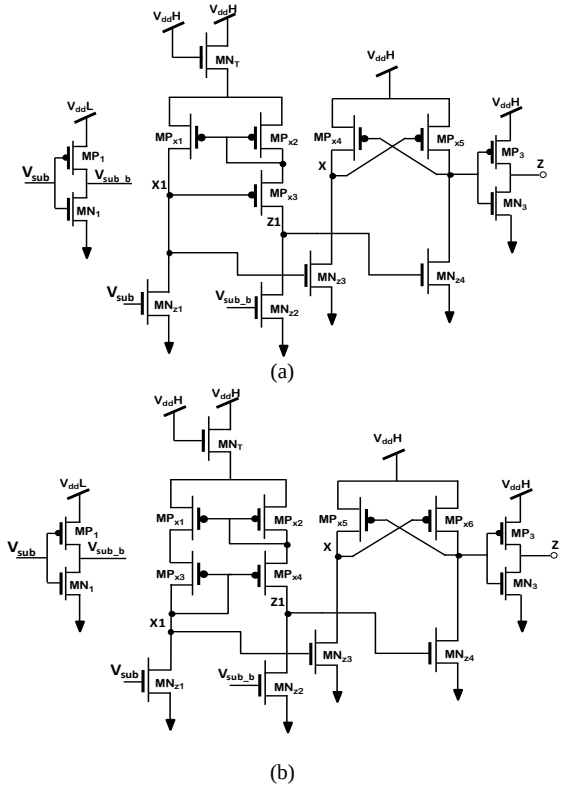
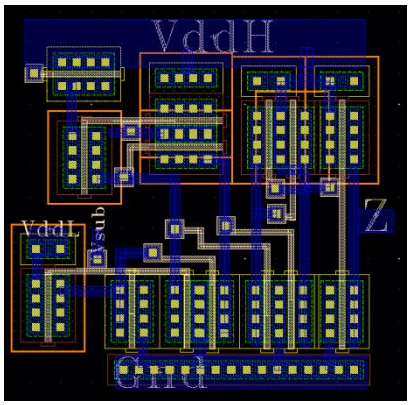


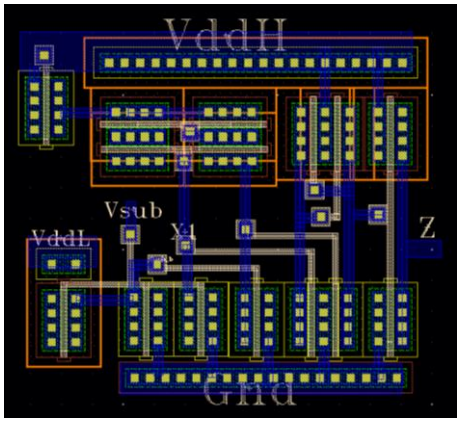
Fig. 3. (a) Proposed Two Stage based level converter with regular Wilson current mirror(PTSW) and**(b)** Proposed Two Stage based level converter with Modified Wilson current mirror(PTSM).

4. Simulation Results

The subthreshold level converter circuits have been implemented in 45nm IBM12SOI Fully Depleted Silicon-On-Insulator (FDSOI) CMOS technology. The large diffusion capacitances associated with the low voltage reverse biasing of the source and drain junctions are virtually eliminated as a result of being implementing in FDSOI technology - well suited for subthreshold operation. The level converter circuits in this study are simulated using HSPICE and tested for operation over a wide range of subthreshold input supply voltage (V_{ddL}), from 250 to 500 mV. The high supply voltage (V_{ddH}) of 1.0 V was chosen as per the device data sheet at 25°C.



(a)



(b)

Fig. 4. (a) Proposed Two Stage based level converter layout with regular Wilson current mirror (PTSW) and **(b)** Proposed Two Stage based level converter layout with Modified Wilson current mirror (PTSM).

Of the conventional circuits, the THL with typical transistor sizings failed to function with subthreshold inputs as the output was held low statically. By increasing the sizings of the NMOS pull-down transistors, the circuits could be designed to work but only at the penalty of unreasonable increase in energy with degradation in performance as well, as shown in Table I, where the THL circuit could only operate at 200 kHz. Conversely, the TCM was fully operational at typical device sizings. For the proposed family of the TCM the circuit naming is based on the number of cascode current mirror employed. For example, the Proposed Cascode Current Mirror (PCCM1) design has one stage of cascode current mirror circuit added to the TCM, and the PCCM2 design has two stages of cascode current mirror added to the basic TCM, and so on, with the final proposed version as PCCM4. Similarly, the analysis for the existing TTS design along with the modified versions of the TTS design - PTSW with regular Wilson current mirror and PTSM with modified Wilson current mirror are included as well.

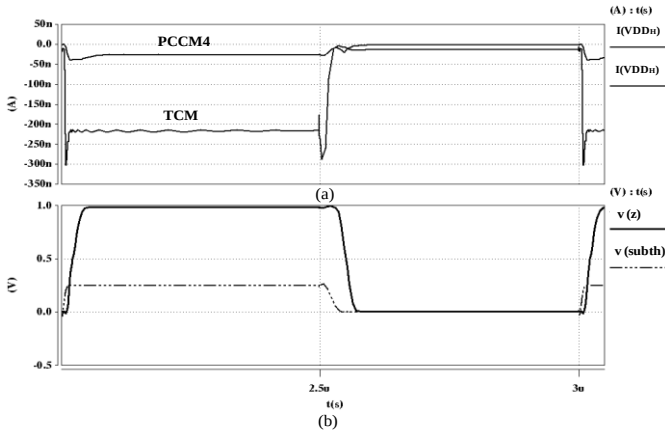


Fig. 5. (a) Current waveform comparison of the TCM with the PCCM4 and (b) Level converter transient simulation

From Table I and Fig. 6, as the number of cascode levels is increased, the total energy decreases by several orders of magnitude due primarily to the increasingly limited current drawn from the V_{ddH} supply. Fig. 3(a) shows the drastic reduction in transient and short-circuit current between the TCM and the proposed four-level cascode, PCCM4. Hence, at 250 mV the total energy consumed by the PCCM4 to perform a single cycle of level conversion (pulsed input with both rise and fall), at 1MHz input frequency is 14.37fJ. In comparison with the TCM, the total energy is reduced by approximately eight times while the delay is increased by only a factor of 1.7. This increase in delay is primarily due to the dramatic reduction in drive strengths of the pull-up PMOS transistors. However, the mild degradation in performance may not be of a concern to applications that operate using energy scavenging techniques, in which improved energy efficiency is more important than performance.

Table I: Level Converter Circuits Comparison

V_{DDL} = 250 mV, V_{DDH} = 1.0 V Subthreshold input signal frequency – 1 MHz *For subthreshold input signal frequency – 200kHz							
Circuit	**# of trans.**	**Total width (µm)**	**Input Cap. (fF)**	**Static Power (µw)**	**Total energy (fJ)**	**Avg. delay (ns)**	**EDP (fj)*(ps)**
THL*	6	20.2	6.3	0.32	1396	221	308
TCM	6	1.2	0.27	0.21	111	15.1	1.68
PCCM1	8	1.4	0.27	0.12	62.4	17	1.06
PCCM2	10	1.6	0.27	0.071	36.9	18.6	0.68
PCCM3	12	1.8	0.27	0.044	23.3	21.4	0.498
PCCM4	14	2.0	0.27	**0.031**	**14.37**	26.7	0.38
TTS	13	2.4	0.27	1.9	715	382	273
PTSW	14	2.6	0.27	0.47	169	22.5	3.8
PTSM	15	2.7	0.27	0.195	118	**2.17**	**0.25**

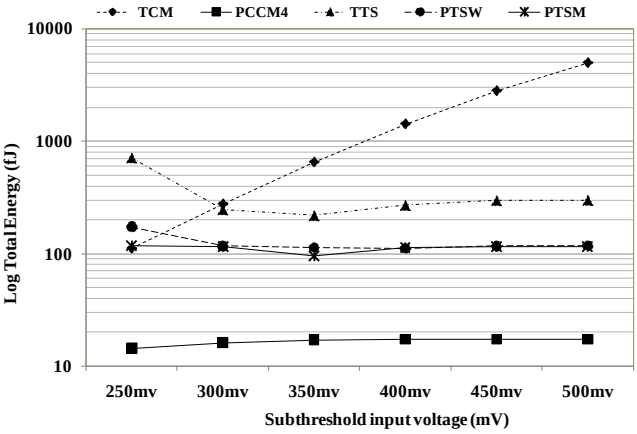


Fig. 6. Logarithmic plot of total energy versus subthreshold supply voltage variation

Alternatively, in cases where performance is the priority, the modified version of TTS - PTSM, can be applied as the delay is reduced by almost seven times compared to TCM for roughly the same amount of energy consumption. For applications that operate with extended periods of inactivity, the PCCM4 provides a better option as the static power dissipation, at 250 mV is reduced by a factor of six compared to TCM and for subthreshold input greater than 300 mV the static power is reduced by approximately two orders of magnitude. In comparison to PTSM, the static power is approximately 6 times lower for the range of subthreshold input voltage.Finally, as shown in Table I the TTS design suffers from severe performance degradation and consumes higher energy because the circuit is evaluated in this study without the suggested multi-threshold devices and subthreshold device sizings, as specified in section 2. The effects are prominent at the lower range of the subthreshold inputs. The first stage half-latch of the TTS has lethargic voltage swings due to the degraded supply voltage and this is compounded by the subthreshold input signal. Consequently, the NFETs struggle to overcome the half-latch PMOS transistors, which results in static leakage increasing dramatically for both stages of the TTS.

However, the proposed versions of the TTS with Wilson current mirrors; PTSW and PTSM, restrict the leakage current with current limiting transistors in the first stage, which not only reduce the drive strength of the PMOS transistors in the half-latch but also improve performance and energy efficiency, as the NMOS transistors can now easily flip the half-latch. The proposed designs are implemented with minimal sizings to demonstrate that

the designs do not require excessively large transistor sizings for the NMOS transistors. Fig. 6 shows that the PCCM4 is clearly the most energy efficient design across the entire input voltage range. Fig. 7 shows that the TCM is the best performer for higher voltages but is overcome by the PTSM at voltages below 380 mV. Finally, the EDP of the proposed PCCM4 and PTSM designs were the best across the entire voltage range.

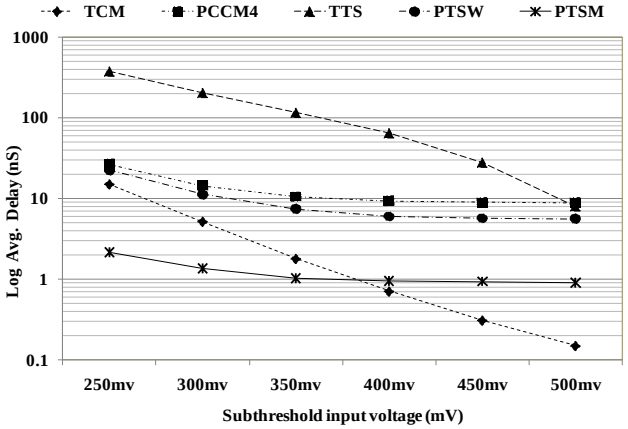


Fig. 7. Logarithmic plot of average delay versus subthreshold supply voltage variation

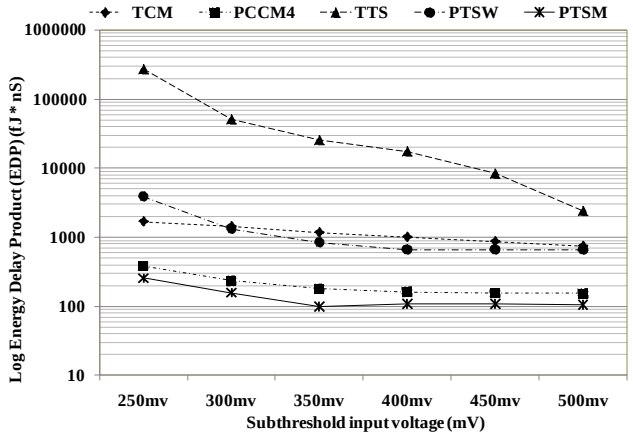


Fig. 8. Logarithmic plot of Energy Delay Product (EDP) versus subthreshold supply voltage variation

5. Conclusion

In this paper for ultra-low power IoT applications, three level converters circuits are proposed and of which two are recommended for subthreshold optimized operation for input levels ranging from 250 to 500 mV. In contrast to existing subthreshold circuits the proposed designs improve power and performance with typical transistor sizings. The first proposed design, PCCM4, improves TCM energy efficiency by several orders for inputs varying over a range of subthreshold to superthreshold levels. Furthermore, the second proposed design, PTSM, enhances performance by several orders for the same input range at similar power levels. Therefore, depending on application requirements, a level converter from the proposed set can be selected to provide optimized energy-performance operation.

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