International Journal of Engineering & Technology, 7 (4) (2018) 2263-2270

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET
doi: 10.14419/ijet.v7i4.12352
Research paper

Design & Optimization of Gate-All-Around Tunnel FET for Low Power Applications

Umesh Dutta [1] *, M. K. Soni [1], Manisha Pattanaik [2]

[1] ECE Department, Faculty of Engineering & Technology, Manav Rachna International Institute of Research and Studies Faridabad, Haryana, Pin code: 121001, India
[2] Department of Information & Communication Engineering ABV-Indian Institute of Information Technology & Management, Gwalior, Pin code: 474015, India
**Corresponding author E-mail: umeshdutta.fet@mriu.edu.in*

Abstract

This paper investigates the performance of tri material gate tunnel field effect transistor (TMGTFET) device designed in gate all around (GAA) configuration. The device performance is analyzed by varying various device related parameters like: drain doping, oxide thickness and radius of silicon core. Simulations are performed using technology computer-aided design (TCAD) tool at 60 nm gate length. Simulation results show that the performance of TMGTFET device can be optimized by proper selection of device parameters so as to achieve improvements in the ON current, OFF current, sub-threshold swing and ambipolar current. The silicon based TMGTFET device demonstrates good performance which makes it a suitable candidate for low power applications with ON current of 0.386 µA/µm, average sub-threshold swing of 32.06 mV/decade, maximum current gain cut off frequency of 41.4 GHz and extremely low OFF current value of the order of 10-20A/µm. We have performed the device optimization to boost the ON current and improve the sub-threshold slope in order to make sure that this device configuration becomes suitable for both low power and high performance applications. The proposed hetero dielectric tri material gate tunnel FET device (HD-TFET) designed in gate all around configuration achieves 19.7 times improvement in ON current as compared to TMGTFET device and excellent average sub-threshold swing of 21.2 mV/decade. The maximum unity current gain frequency is also improved by 3 times indicating its potential for deployment in high frequency applications.

Keywords: *TFET; Technology Computer-Aided Design Simulation (TCAD); Band to Band Tunneling (BTBT); Subthreshold Slope; High-K Dielectric; Am bipolar Current.*

1. Introduction

Scaling of the device dimensions in MOSFETs has led to various challenges like enhancement in the short channel effects (SCEs), increase in the leakage current and reliability issues which needs to be addressed in order to ensure better performance of the VLSI circuits under low voltage operation. MOSFETs sub-threshold slope is limited by Boltzmann distribution of carriers to 60 mV/decade of the channel current at room temperature [1]. The sub-threshold slope of silicon tunnel field-effect transistors (TFETs) at room temperature can be reduced to less than 60mV/decade which makes it a promising device for applications requiring LSTP operation [2]. Apart from the possibility of low sub-threshold swing these TFET devices have the potential for achieving extremely low OFF current [3, 4]. Lower ON current in TFETs is a major concern primarily because of the use of indirect and large band gap semiconductor material for TFET fabrication [1-5]. A novel double gate tunnel FET (DGTFET) with high-K dielectric was proposed in [3] which showed high ON current of 0.23 mA at a gate voltage of 1.8V with extremely low OFF current value of less than 1fA. Jhaveri et al. [6] used dopant engineering technique by creating a source pocket to enhance the ON current of the TFET device. ON current enhancement can also be achieved by using low energy band gap material (such as Ge, SiGe, InAs, InGaAs) for the TFET fabrication [7]. Vertical TFET design proposed in [8] can lead to ON current enhancement because of increase in the tunneling area as compared to lateral TFET device. Ambipolar conduction is another important issue in TFET and this comes into picture when TFET device conducts current for both the higher value of positive and negative gate source voltage. Underlapping and overlapping of the gate on drain can suppress the ambipolar conduction to a great extent [9-10]. Gate all around tunnel FET has better gate to channel control and hence it possesses better short channel performance than those with single or double gate structures [11-12]. Improvement in the sub-threshold slope and Ion/Ioff ratio of GAATFET device can be achieved by underlapping the drain junction [13]. Zhang et al. [14] performed the comparative analysis of single material gate and dual material gate tunnel FET designed in gate all around configuration and reported that DMG-TFET device has lower leakage and comparative ON current as compared to SMGTFET device. The experimental demonstration of strained Si nanowire GAA n-TFET has been reported in [15]. Wang et al. [16] proposed a novel barrier controlled TFET device in gate all around configuration which has triple material gate and results reported show that this configuration can lead to enhancement of ON current due to band bending at the source side with the added benefit of reduction in the OFF current due to the effective band pass filtering with the in channel barrier.

The rest of the paper is organized as follows: Section II describes the design of TMGTFET device in gate-all-around configuration and also highlights the Kane's band to band tunneling model used in TCAD tool for performing device simulations. Section III highlights various important performance metrics of the TFET device.

Parameter variation study of the TMGTFET device is discussed in section IV. Optimized HD-TFET device design and its analysis is performed in Section V. Comparative study of the HD-TMGTFET device and TMGTFET device is done in section VI to analyze the RF and analog performance and finally in section VII conclusions are drawn.

2. GAA TFET device architecture and KANE'S BTBT model

Gate-all-around Tunnel FET (GAA-TFET) exhibits excellent ON current to OFF current ratio and this is achieved due to the excellent electrostatic control of gate over the channel. GAA-TMTFET device schematic is shown in Fig. 1.

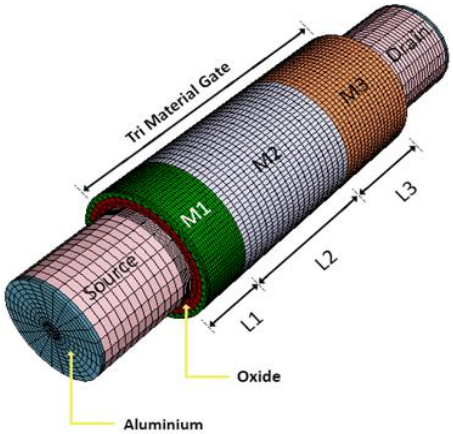

Fig. 1: TMGTFET device in gate all around configuration.

The device dimensions, doping concentration of different regions and work function of different segments of the gate are highlighted in Table I. Gate is composed of three different segments labeled as M1, M2 and M3 with lengths of L1, L2 and L3 respectively. The work function of segment M1 (ϕ_1) and M3 (ϕ_3) is kept lower than the work function of segment M2 (ϕ_2). A lower value of ϕ_1 increases the band bending and electric field at the source-channel junction [16], while a higher value of ϕ_2 creates an in channel barrier. Lower ϕ_3 value acts as a band pass filter making this configuration a barrier controlled TFET (BC-TFET) where barrier is formed by gate metal work function engineering. The doping of the source and drain region is kept asymmetric in order to suppress the ambipolar characteristics because lower drain doping increases the width of the depletion layer on the drain side which suppresses the ambipolar conduction in TFET device[9]. The transfer characteristics and band diagram of GAA-TMGTFET device are shown in Fig. 2(a) and Fig. 2(b) respectively. It is clear from the band diagram profile that there is a formation of an in channel barrier due to the work function difference of the gate material segments. In the off state (defined as V_{gs} = 0V and V_{ds} = V_{dd} , V_{dd}=1V in this case) the barrier height is more which blocks the movement of charge carriers across the source-channel junction and hence the off state current of the TFET device is extremely low. When the gate to source voltage is made positive then energy band gap modulation takes place. A higher positive gate to source voltage narrows the tunneling barrier width at the source-channel interface thereby enhancing the tunneling probability and this leads to increase in the drain current of the device.

GAA-TMGTFET device is designed using Cogenda Visual TCAD tool and Kane's Local band-to-band tunneling model [17] is used in the simulations. When electric field is uniform across the entire tunneling region Kane's model can be used to determine the BTBT generation rate per unit volume and it is given by:-

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_g}}\exp\left(-B.BTBT.\frac{E_g^{3/2}}{E}\right) \quad (1)$$

where E is the electric field, A.BTBT and B.BTBT are Kane's parameters, E_G is the energy band gap. The advantage of using local tunneling model is that it is fairly accurate and for 3D devices simulation convergence is also better. SRH model for carrier recombination and Fermi-Dirac statistics are also invoked during simulation. Parameters A.BTBT and B.BTBT are tuned to match the experimental data reported in [15]. The drain current Id is obtained by integrating the BTBT generation rate given in equation (1) over the entire volume of the device: -

$$I_{ds} = q\int G^{BB} dV \quad (2)$$

Table 1: GAA-TMGTFET Device Parameters

Parameter	Value
Source doping (Na in Cm^{-3})	1e20
Drain doping (Nd in Cm^{-3})	1e17
Channel doping (Nch in Cm^{-3})	1e16
Oxide Thickness (tox in nm)	2
Gate Length (Lg in nm)	60
Length of source/drain (nm)	20
Radius of Silicon body (nm)	10
Gate Work Function (ϕ_1, ϕ_2, ϕ_3) in eV	
ϕ_1-Silver (Ag), ϕ_2-Tungsten (W), ϕ_3-Copper (Cu)	4.4, 4.8, 4.6
Gate Length in nm (L1, L2, L3)	10,30,20

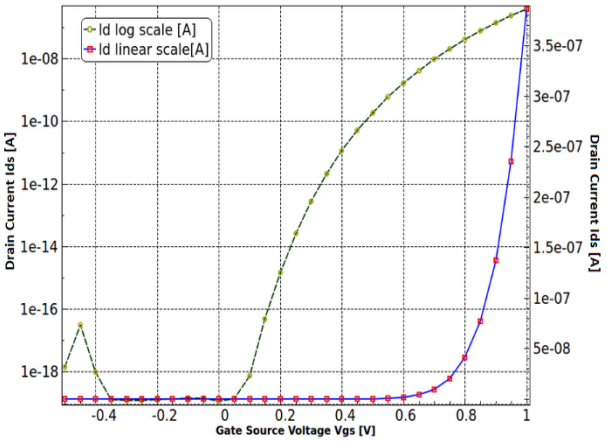

Fig. 2(a): Transfer characteristics plot of TMGTFET device.

3. Performance metrics

The performance of the TFET device will be observed by measuring various important performance metrics that are important from both analog and digital applications point of view. They are described below:-

ON current and OFF current

On-current of the TFET device considered in this work is the drain current I_{ds} at V_{gs} = 1V with V_{ds} =1V. OFF current is the drain current value at V_{gs} = 0V with V_{ds} = 1V. In order to use TFET device in low power high performance (LPHP) applications it should have high ON current to OFF current ratio.

Sub-threshold Swing

It is the amount of gate voltage which must be applied with respect to source so as to increase the drain current by one decade [18-19]. Sub-threshold swing in TFET is expressed as:

$$Subthreshold\ \ Swing = \frac{dVg}{d(\log Id)} mV\ /dec. \quad (3)$$

Tunneling current in TFET device is given by [1,19]-

$$I_{ds} = aV_{eff}\xi \exp\left(\frac{-b}{\xi}\right) \quad (4)$$

where coefficients a & b in equation (4) are determined by material properties and area of device. They are expressed as: -

$$a = \frac{Aq^3\sqrt{2m^*/E_g}}{4\Pi^2\hbar^2} \quad \text{and} \quad b = \frac{4\sqrt{m^*}E_g^{3/2}}{3q\hbar}$$

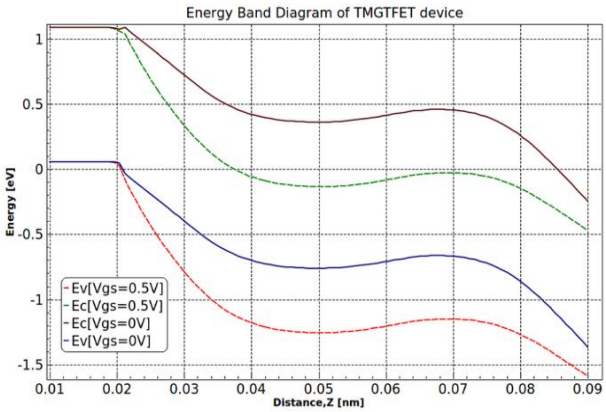

Fig. 2(b): Energy band diagram of GAA-TMGTFET device.

where q is the charge of electron, E_g is energy band gap, $\hbar$ is Planck's constant, m^* is the carrier effective mass. Simplified expression derived from equation (3) for calculating the sub-threshold swing is given by: -

$$SS = \ln(10)\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{gs}} + \frac{\xi + b}{\xi^2}\frac{d\xi}{dV_{gs}}\right]^{-1} \quad (5)$$

where V_{eff} represents tunnel junction bias, ξ is the junction electric field. SS value of less than 60mV/dec at 300K has been achieved in Si based nano wire gate all around TFET. Equation (5) indicates that in order to maximize the subthreshold swing the TFET device should be engineered in such a way so that the gate bias voltage directly controls the tunnel junction bias Veff. The other way to improve the slope is to maximize the derivative of junction electric field with respect to gate source voltage. Average sub-threshold swing is proposed by Boucart et al. [2]: -

$$SS_{avg} = \frac{V_{th} - V_{off}}{\log\left(\frac{I_{th}}{I_{off}}\right)} \quad (6)$$

where V_{th} is the threshold voltage and it is extracted using constant current method. It is the gate source voltage at which the drain value is 10^{-7} A/μm. I_{th} is the drain current at $V_{gs} = V_{th}$ and I_{off} is the drain current value at $V_{gs} = V_{off}$

Unity gain frequency

It is the frequency at which the short circuit current gain of the device falls to unity [2]. It is expressed as:-

$$f_T = \frac{g_m}{2\Pi(C_{gs} + C_{gd})} \quad (7)$$

where C_{gs} and C_{gd} are miller capacitance's of TFET device.

Transconductance generation efficiency

This is another important performance metric that represents available gain per unit of power dissipation [21]. It is also termed as device efficiency and it is one of the very important parameters for analog design application. Device efficiency of a TFET device can be expressed as: -

$$Device\ Efficiency = \left(\frac{g_m}{I_{ds}}\right) \quad (8)$$

Transit time

It is the time taken by the charge carriers (electrons) to cross the channel. Analytical expression for calculating the transit time as expressed in [20] is-

$$\tau = \frac{1}{2\Pi f_T} \quad (9)$$

4. Parameter variation study

In this section a detailed parameter variation study of the TMGTFET device will be performed. The impact of the variation in drain doping concentration, oxide thickness and radius of the silicon core on the device performance is analyzed in order to select the optimum parameter values so as to achieve excellent performance in terms of ON current, OFF current and sub-threshold slope.

a) Variation in the drain doping concentration

Ambipolarity is a severe issue in TFETs and it becomes quite obvious to analyze the TMGTFET device designed in gate all around configuration from this point of view. Different drain doping concentrations are considered and its impact on the ambipolar current is seen. Fig. 3 shows the transfer characteristics curve under the drain doping concentration variation. Ambipolar current considered here is the value of the drain current at V_{gs} = -0.5 V with V_{ds} = 1V. It is clear from Fig. 3 that ambipolar current is reduced to less than 10^{-17} A/μm when the drain doping is reduced to 1e17 cm^{-3}. The prime reason for the reduction in the ambipolar current with the reduction in drain doping is due to increase in the width of the depletion region on the drain end. It is as evident from Fig. 4 that the electric field at the drain end increases with increase in the drain doping concentration which increases the tunneling rate at higher negative value of gate to source voltage. TFET device designed using lower drain doping generally has lower ON current but this issue of poor ON current can be addressed by using device engineering techniques that can boost the ON current of a TFET device.

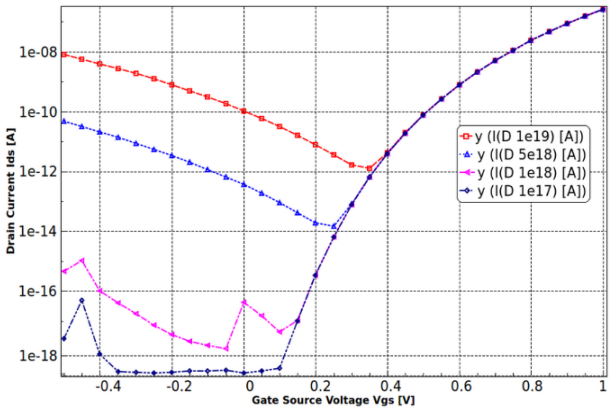

Fig. 3: Transfer characteristics plot under different drain doping concentration

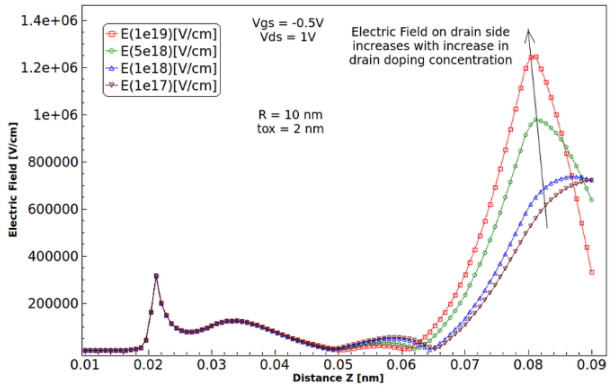

Fig. 4: Electric field plot at various drain doping concentration.

b) Variation in the oxide thickness

Oxide thickness affects the ON current of the device significantly as change in the oxide thickness leads to change in the vertical electric field across the source-channel junction. Different oxide thickness values considered in the simulation are: 2nm, 4nm, 6nm, 8nm and the drain doping is kept at 1e17 cm^{-3} so as to keep the ambipolar current to significantly low value. Fig. 5 and Fig. 6 shows the transfer characteristics and the energy band bending effect that is seen across the source-channel junction under the oxide thickness variation. It is clear from Fig. 6 that in case of oxide thickness of 2 nm the band bending is more as compared to any other value of oxide thickness considered in the simulation. This band bending leads to reduced barrier width across the source-channel junction which increases the tunneling rate of the electrons thereby leading to enhancement in the drain current of the device.

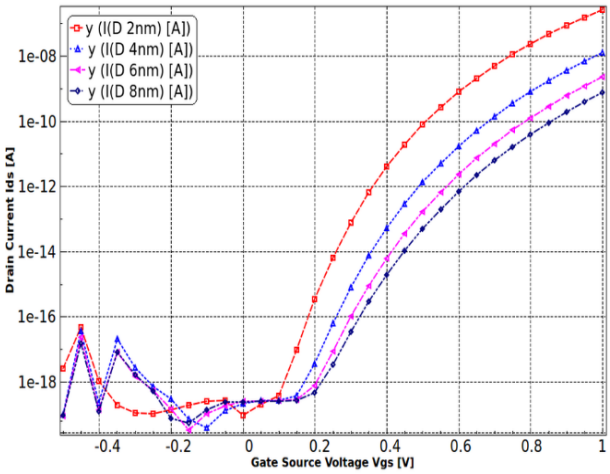

Fig. 5: Transfer characteristics plot under oxide thickness variation.

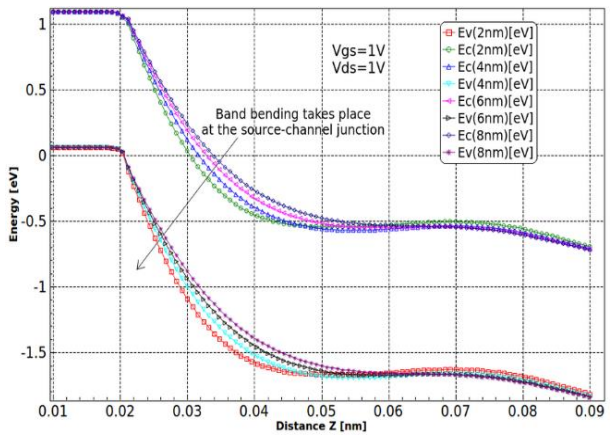

Fig. 6: Energy band diagram under oxide thickness variation.

c) Variation in the radius of silicon core

The radius of the silicon core is another important parameter that can significantly affect the performance of TFET device. Different radii values that are considered for simulation study are: 10nm, 8nm and 6nm. Fig. 7 and Fig. 8 show the transfer characteristics and lateral electric field plot under the variation in the radius of the silicon core. Lower radii value increases the lateral electric field across the source-channel interface which increases the tunneling probability of the electrons. Peak electric field value of 1.84 MV/cm is obtained at 6 nm silicon core radius which is 34.3% higher as compared to the electric field value achieved at silicon radius value of 10 nm. It can be observed from Fig. 5 and Fig. 7 that it is the oxide thickness, which causes a significant change in the transfer characteristics of TFET device as compared to variation in the radius of the silicon core. The ON current enhancement is not much when radius value is called from 10 nm to 6 nm. The OFF current is less than 10^{-18} A/μm and the device exhibits excellent sub-threshold slope of 32.06 mV/decade. From the above parameter variation study it becomes quite clear that correct selection of device parameters is extremely important to optimize the performance of a TFET device.

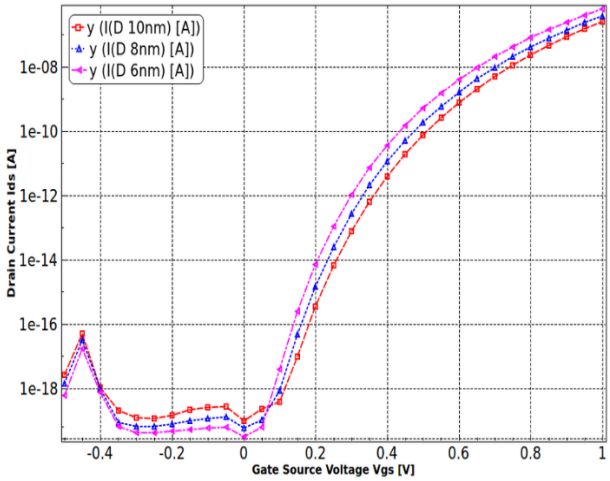

Fig .7: Transfer characteristics plot under Si-core radii variation.

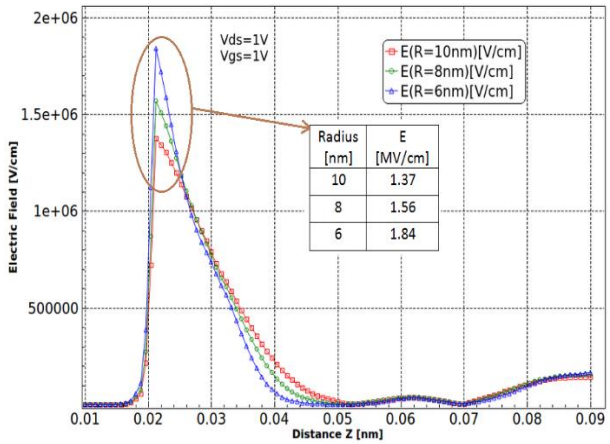

Fig. 8: Lateral electric field variation with radius scaling.

ON current and sub-threshold slope enhancement can be achieved by using TFET device with smaller oxide thickness and narrow silicon radius. Ambipolarity reduction can be achieved by lowering the drain doping concentration but this method surely poses a challenge for the device engineers to use some other way to enhance the ON current of the device so that they can be suited for deploying in low power and high performance applications. In the next section the problem of lower ON current in GAA-TMGTFET device will be addressed by using hetero dielectric configuration rather than using SiO_2 alone as dielectric.

5. Optimized HD-TMGTFET device

In order to enhance the ON current and sub-threshold slope the design of the GAA-TMGTFET device is modified and a high-K dielectric is introduced beneath the gate metal M1. This enhances the ON current of the TFET device. HD-TFET device is designed using the same device parameters as highlighted in Table I at 8 nm silicon radius. As seen in the previous section the change in the TFET device performance is not much improved by the change in the radius of the silicon core so we have taken 8 nm silicon radii for the simulation of HD-TMGTFET device. Fig. 9 shows the schematic diagram of HD-TMGTFET device designed in gate all around

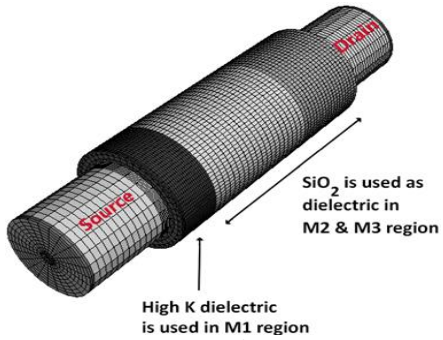

Fig. 9: Schematic diagram of HD-TMGTFET device.

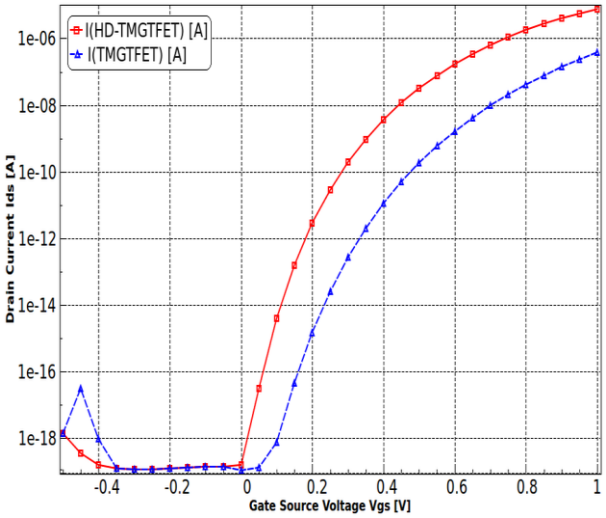

Fig. 10: Transfer characteristics comparison plot.

Configuration. The comparative transfer characteristics plot is shown in Fig. 10. It is quite clear from Fig. 10 that the proposed HD-TMGTFET device exhibits higher ON current and steep sub-threshold swing as compared to the conventional TMGTFET device. The enhancement in the ON current of the HD-TFET device is because of the increase in the magnitude of the lateral electric field across the tunneling junction at the source channel interface which leads to reduction in the energy band gap at the source-channel interface in HD-TMGFET device. High-K dielectric material (Si_3N_4) with dielectric constant of 7.5 is used in the simulation. Fig. 11 below shows the electric field intensity variation along the channel length clearly showing the increase in the peak electric field value in HD-TFET device. The band gap reduction with increase in the gate to source voltage observed in HD-TFET device is shown in Fig. 12. The ON current enhancement of 19.7 times is achieved in HD-TMGTFET device as compared to the conventional GAA-TMGTFET device designed using 8 nm silicon core.

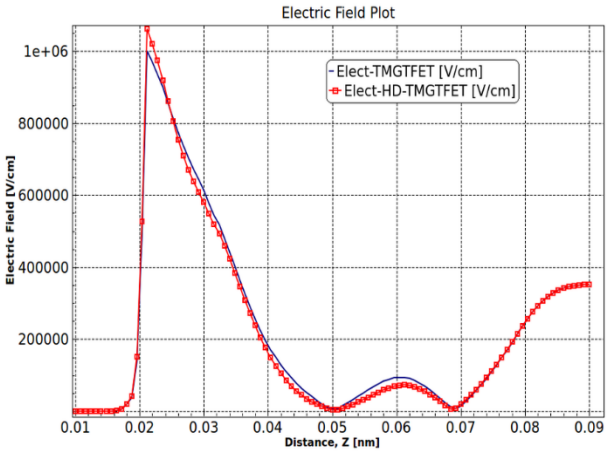

Fig. 11: Lateral electric field comparison plot.

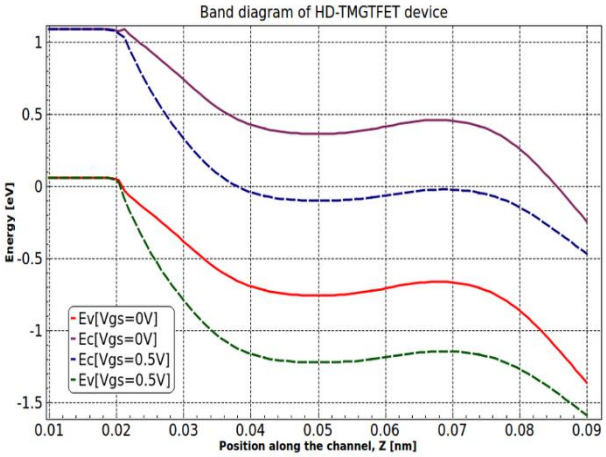

Fig. 12: Band diagram of HD-TMGTFET device.

The ON current enhancement of 19.7 times is achieved in HD-TMGTFET device as compared to the conventional GAA-TMGTFET device designed using 8 nm silicon core. The average subthreshold swing of the HD-TMGTFET device calculated using equation (4) is also improved to 21.6 mV/decade showing 33.8% improvement as compared to TMGTFET device without causing much degradtion in the OFF current. The proposed HD-TMGTFET device also possess higher transconductance as evident from Fig. 13 and Fig. 14. The above facts indicate that the proposed HD-TMGTFET device is a better candidate for replacing MOSFET in LPHP applications. In order to analyze the TFET device from analog and RF performance point of view it becomes necessary to extract the miller capacitances ie. gate-source capacitance (C_{gs}) and gate- drain capacitance (C_{gd}). Total gate capacitance (C_{gg} = C_{gs}+C_{gd}) [22] has to be low and transconductance (g_m) of TFET device should be high in order to achieve better RF performance as evident from equation (5).

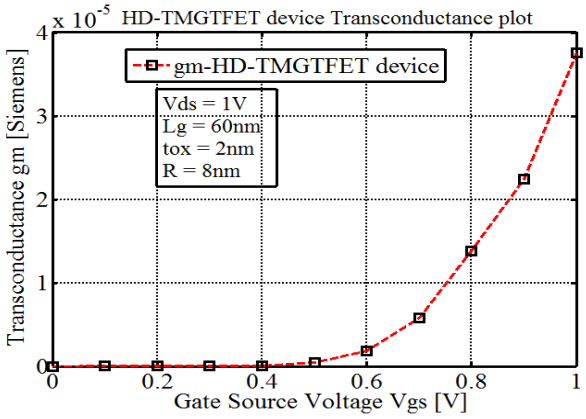

Fig. 13: Transconductance Plot of HD-TMGTFET device.

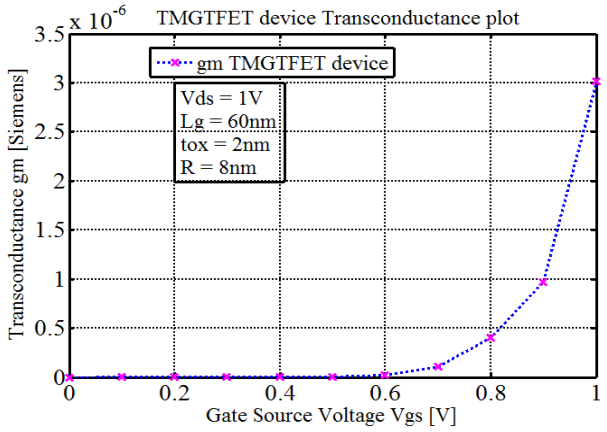

Fig. 14: Transconductance plot of TMGTFET device.

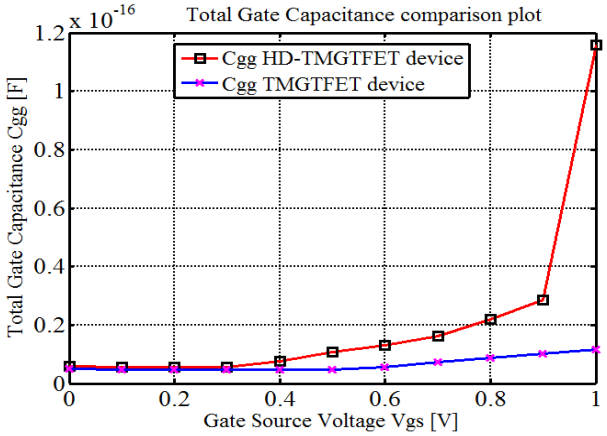

Fig. 15: Total gate capacitance plot.

6. RF and analog performance analysis

In order to analyze the RF performance of the device a 1MHz source is applied at the gate terminal which is ramped from 0 to 1.0 V and miller capacitance values (C_{gs} and C_{gd}) are extracted. These capacitance values are used along with transconductance (g_m) to evaluate an important RF figure of merit known as the cut off frequency (f_T) of the TFET device as mentioned in equation (7). C_{gd} and C_{gs} are intrinsic gate-drain and gate-source capacitance values respectively and in a TFET device it is gate-drain capacitance which has more contribution in the total gate capacitance (Cgg) [2], [22], [23]. Fig. 15 shows the total gate capacitance comparison plot which indicates that in the proposed HD-TMGTFET device there is an increase in the total gate capacitance as compared to TMGTFET device. The extent of increase in the total gate capacitance in case of HD-TMGTFET device is not much significant upto the gate source voltage of 0.9 V and beyond that the increase in the total gate capacitance is quite significant which will ultimately decrease the cut off frequency at gate-source voltage beyond 0.9 V. Fig. 16 shows the comparative plot of the unity gain frequency of HD-TMGTFET device and conventional TMGTFET device designed in gate all around configuration. Unity gain frequency is 41.2 GHz at Vgs value of 1.0 V and in case of HD-TMTFET device the maximum unity gain frequency of 124 GHz is obtained at 0.9 V. The prime reason for the increase in the f_T value upto Vgs value of 0.9 V is due to increase in transconductance (g_m) of HD-TMGTFET device and also the fact that total gate capacitance does not increase significantly up-to the gate source voltage range of 0-0.9 V. The unity gain frequency dip seen at V_{gs}=1V is due to the sharp rise in the total gate capacitance of the device. Another important figure of merit to analyze the RF performance is the transit time which is calculated using equation (9).

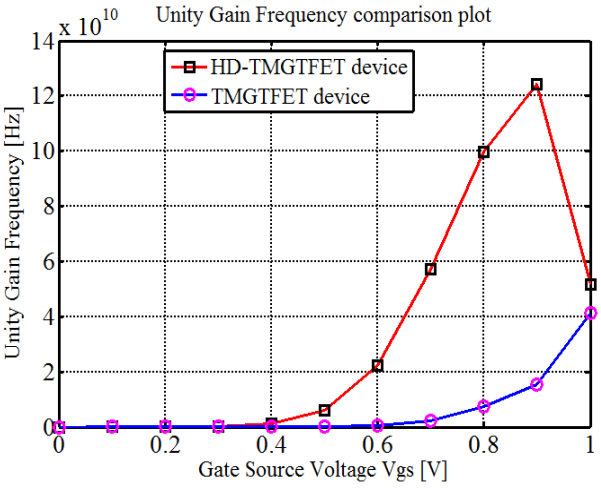

Fig. 16: Unity gain frequency comparison plot.

This parameter is used to determine the speed of the device. Since transit time is inversely proportional to unity gain frequency, so the proposed HD-TMGTFET device possess lower value of transit time indicating its potential for use in applications which need high speed of operation like memory design. In order to analyze the analog performance of the device various important analog performance parameters are extracted which includes: device efficiency and output resistance. Device efficiency is extracted using equation (8) and comparative analysis reveals that device efficiency is maximum at lower drain current and it decreases with the increase in the drain current. Maximum device efficiency that can be achieved in case of a MOSFET operating near sub-threshold region is around 40 V^{-1}.

Table 1: Performance Comparison Matrix

Device Topology	Threshold Voltage [V] [Constant Current method]	OFF current [A/μm]	ON current [A/μm]	Sub threshold swing [mV/dec]	Trans conductance g_m [Siemens]	Output resistance [Ro = 1/gds] @V_{gs}=1V [Ohm]	Miller Capacitance C_{gs} [F/μm]	Miller Capacitance C_{gd} [F/μm]	Max. Cut off frequency f_T [GHz]
TMGTFET device	0.9	8.88E-20	3.86E-07	32.06	3.014E-06	3.70E+08	3.29E-18	8.29E-18	41.4 @ V_{gs}=1V
HD-TMGTFET device	0.6	2.20E-19	7.50E-06	21.92	3.75E-05	2.39E+06	6.86E-18	1.09E-16	124 @V_{gs}=0.9V

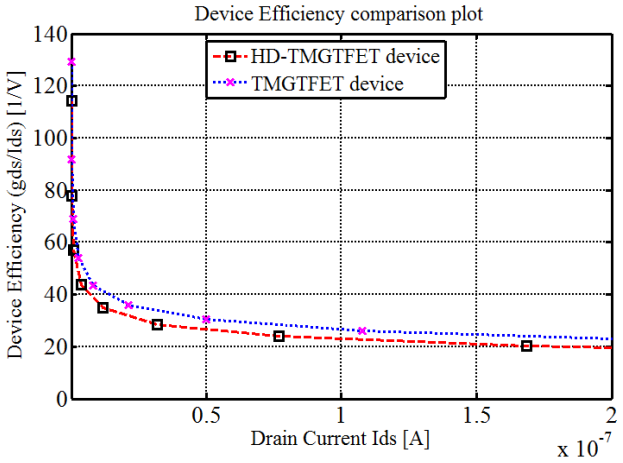

Fig. 17: Device efficiency comparison plot.

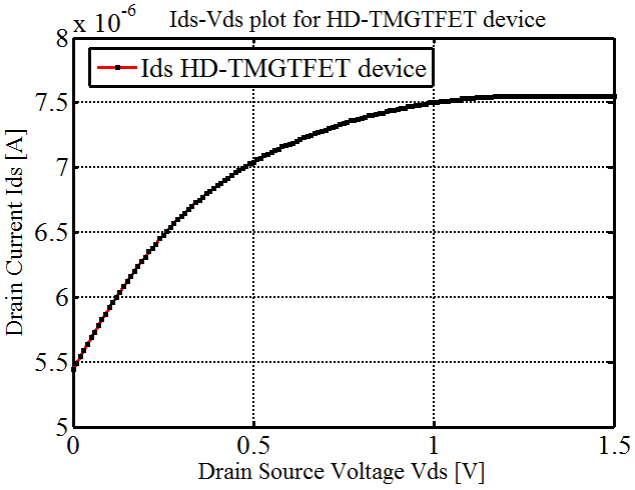

Fig. 18: Output characteristics plot of HD-TMGTFET device.

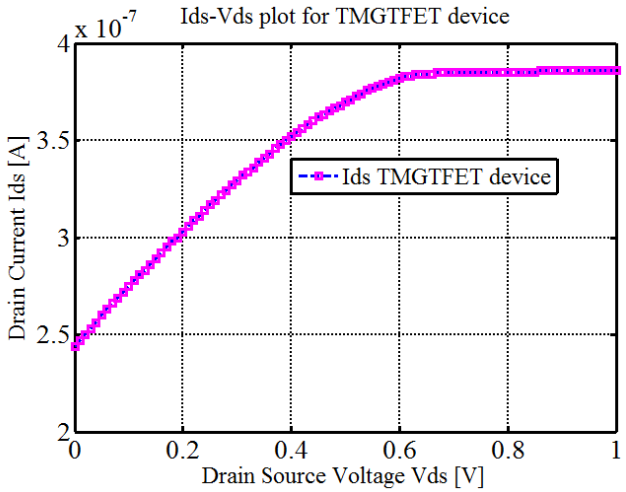

Fig. 19: Output characteristics plot of TMGTFET Device.

Fig. 17 shows the device efficiency comparison plot which shows that device efficiency in case of HD-TMGTFET is 57.0 V^{-1} at I_{ds} value of the order of 10^{-10}A and in case of TMGTFET device it is 68.9 V^{-1}. This signifies that both TMGTFET and HD-TMGTFET device has higher gain as compared to MOSFET near the sub-threshold region. The output resistance of the TFET device is calculated using I_{ds}-V_{ds} output characteristics curve. The drain transconductance (g_{ds}) is extracted and the output resistance is calculated by taking the reciprocal of the drain transconductance (ie. Ro = 1/gds). Fig. 18 and Fig. 19 shows the output characteristics of HD-TMTFET device and conventional TMGTFET device respectively. It is quite clear from output characteristics curve that if the drain voltage is increased beyond the drain threshold voltage point then the drain current increases at a much lower pace particularly because of the increase in the channel resistance. The dependence of I_{ds} on V_{ds} eventually ends at higher V_{ds} value and this indicates that tunneling barrier width cannot be reduced further by increasing the drain voltage and this leads to saturation in the drain current. It can be seen in the output characteristics plot that the proposed HD-TMGTFET device shows delayed saturation effect which means that the pinch off point shifts on the higher drain potential at a higher value of gate to source voltage. The output resistance in both the configurations is very high which will ensure higher intrinsic (g_mRo) gain that can be achieved in the TFET device. The output resistance has dropped to almost 100 times as compared to conventional TMGTFET device due to increase in the drain current which occurs primarily due to drain induced barrier thinning (DIBT). Enhanced g_m value and high output resistance ensures high intrinsic gain of the device which is extremely important for any device to be deployed for analog applications like a common source amplifier circuit. Literature also suggests that TFET devices can be used in designing reliable and low power applications like SRAM, DRAM and inverter circuit [24-26]. Unlike MOSFETs, TFETs exhibit unidirectional conduction because of their asymmetric source and drain architecture [24, 27]. This unidirectional behaviour causes a lot of challenges for the circuit designers to design area efficient high-performance circuits. Miller capacitance and interface trap charges can severely affect the performance of the TFET device [28-29]. Despite various challenges the research work carried out in the last two decades on TFET device shows that TFET device holds a promising future in designing VLSI circuits [30]. Use of low energy band gap materials in TFET device design can further optimize its performance in terms of achieving ON current of the same order as that of a MOSFET.

7. Conclusion

In this paper the detailed study of the effect of parameter variation on the performance of tri material gate tunnel FET (HD-TMGTFET) device has been performed. It is observed that drain doping is an important parameter which affects the ambipolar conduction of the TFET device and lower drain doping will ensure lower level of ambipolar conduction. Radius of the silicon core does not affect the device performance significantly as compared to the oxide thickness. Lower oxide thickness boosts the ON current of the device primarily because of band lowering observed at the source channel interface. The triple material gate all around TFET device topology uses three different work functions for the gate metal and this is an added advantage for the device engineers to tune the device performance. The ON current boosting can be achieved by the introduction of high-K dielectric material beneath the gate metal at the source channel interface. This proposed design of HD-TMGTFET device achieved an ON current boosting of 19.7 times as compared to conventional TMGTFET configuration primarily because of reduction in the barrier width at the source-channel junction. The impact on the analog and RF performance is also analyzed by extracting various important performance parameters. The investigation results reveal that the proposed HD-TMGTFET device achieves better RF performance with an increase in the unity gain frequency to around 3 times as compared to the maximum unity gain frequency value that can be achieved in TMGTFET device. The maximum f_T value achieved in case of HD-TMGTFET device is 124 GHz. This increase in the unity gain frequency along with reduction in the intrinsic delay makes the proposed HD-TMGTFET device a suitable candidate for use in low power high performance VLSI circuits.

Acknowledgment

The authors would like to thank the management of Manav Rachna Educational Institutions for providing research facilities for carrying out this work. Authors would also like to acknowledge the time devoted by the technical team from Cogenda and Cadre Design Systems for the discussions that are carried out on the subject matter.

References

[1] A. C. Seabaugh, and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic," *Proceedings of the IEEE*, vol.98, no. 12, pp. 2095-2110,Dec.2010. https://doi.org/10.1109/JPROC.2010.2070470.

[2] Seongjae Cho, Jae Sung Lee, Kyung Rok Kim, Byung-Gook Park, James S. Harris and In Man Kang, "Analyses on Small – Signal Parameters and Radio-Frequency Modeling of Gate-All-Around Tunneling Field Effect Transistors," *IEEE Transactions on Electron Devices*,vol.58,no.12,pp.4164-4171,Dec.2011. https://doi.org/10.1109/TED.2011.2167335.

[3] K. Boucart, and A. M. Ionescu, "Double-Gate Tunnel FET with High-k Gate Dielectric," *IEEE Trans. on Electron Devices*, vol.54, no.7,pp.1725-1733,Jul.2007. https://doi.org/10.1109/TED.2007.899389.

[4] R. Jhaveri, V. Nagavarapu, and J.C.S. Woo, "Effect of Pocket Doping and Annealing Schemes on the Source- Pocket Tunnel Field- Effect Transistor," *IEEE Trans. on Electron Devices*, vol. 58, no. 1, pp. 80-86, Jan. 2011. https://doi.org/10.1109/TED.2010.2089525.

[5] Giovanni Betti Beneventi, Elena Gnani, Antonio Gnudi, Susanna Reggiani and Giorgio Baccarani, "Dual-Metal-Gate InAs Tunnel FET With Enhanced Turn-On Steepness and High ON-Current," *IEEE Transactions on Electron Devices*, vol.61, no.3, pp.776-784, Mar. 2014. https://doi.org/10.1109/TED.2014.2298212.

[6] R. Jhaveri, V. Nagavarapu, and J.C.S. Woo, "Effect of Pocket Doping and Annealing Schemes on the Source- Pocket Tunnel Field- Effect Transistor," *IEEE Trans. on Electron Devices*, vol. 58, no. 1, pp. 80-86, Jan. 2011. https://doi.org/10.1109/TED.2010.2089525.

[7] H. Liu, S. Dutta, *III-V Tunnel FET model manual*, 2015,[online]Available:https://nanohub.org/publications/12/2.

[8] S. Agarwal, G. Klimeck, and M. Luisier, "Leakage- Reduction Design Concepts for Low-Power Vertical Tunneling Field- Effect Transistors," *IEEE Electron Device Letters*, vol. 31, no. 6, pp. 621-623, Jun. 2010. https://doi.org/10.1109/LED.2010.2046011.

[9] Dawit B.Abdi and M.Jagadesh Kumar, "Controlling Ambipolar Current in Tunneling FET's using Overlapping Gate-on Drain," *Journal of the Electron Devices Society*, vol.2, no.6, pp.187-190, Nov. 2014. https://doi.org/10.1109/JEDS.2014.2327626.

[10] C. Anghel, Hraziia, A. Gupta, A. Amara and A. Vladimirescu,"30-nm Tunnel FET With Improved Performance and Reduced Ambipolar Current," *IEEE Trans. on Electron Devices*, vol. 58, no. 6,pp.1649-1654,Jun.2011. https://doi.org/10.1109/TED.2011.2128320.

[11] Jun-Sik Yoon, Kihyun Kim, Taiuk Rim and Chang-Ki Baek, "Performance and Variations Induced by Single Interface Trap of Nanowire FET's at 7-nm Node," *IEEE Transactions on Electron Devices*,vol.64,no.2,pp.339-344,Feb2017. https://doi.org/10.1109/TED.2016.2633970.

[12] Chunsheng Jiang, Renrong Liang and Jun Xu, "Investigation of Negative Capacitance Gate-all-around Tunnel FET's Combining Numerical Simulation and Analytical Modeling," *IEEE Transactions on Nanotechnology*, vol.16, issue 1, pp.58-67, Jan 2017.

[13] Jae Sung Lee, Jae Hwa Seo, Seongjae Cho, Jung- Hee Lee, Shin-won Kang, Jin-Hyuk Bae, Eou-sik Cho and In Man Kang, "Simulation study on effect of drain underlap in gate-all-around tunneling field-effect transistors," 2013, *Current Applied Physics*,13(6), pp. 1143-1149. https://doi.org/10.1016/j.cap.2013.03.012.

[14] A. Zhang, J. Mei, L. Zhang, H. He, J. He and M. Chan, "Numerical study on dual material gate nanowire tunnel field-effect transistor", *IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC)*, 2012, pp.1 - 5.

[15] Z. X. Chen, H. Y. Yu, N. Singh, N. S. Shen, R. D. Sayanthan, G. Q. Lo and D. L. Kwong, "Demonstration of Tunneling FETs Based on Highly Scalable Vertical Silicon Nanowires," *IEEE Electron Device Lett.*,vol.30,no.7,pp.754-756,Jul.2009. https://doi.org/10.1109/LED.2009.2021079.

[16] Hao Wang, Sheng Chang, Yue Hu, Hongyu He, Jin He, Qijun Huang, Frank He and Gaofeng Wang, "A Novel Barrier Controlled Tunnel FET," *IEEE Electron Device Letters*, vol.35, no.7, pp.798-800, Jul. 2014. https://doi.org/10.1109/LED.2014.2325058.

[17] Kuo-Hsing Kao, Anne S. Verhulst, William G. Vandenberghe, Bart Soree, Guido Groeseneken and Kristin De Meyer, "Direct and Indirect Band-to-Band Tunneling in Germanium-Based TFET's," *IEEE Transactions on Electron Devices*, vol.59, no.2, pp.292-300, Feb.2012. https://doi.org/10.1109/TED.2011.2175228.

[18] Umesh Dutta, M.K.Soni, Manisha Pattanaik, "Design and Analysis of Tunnel FET for Low Power High Performance Applications", *International Journal of Modern Education and Computer Science (IJMECS)*,vol.10,no.1,pp.65-73. https://doi.org/10.5815/ijmecs.2018.01.07.

[19] Qin Zhang, Wei Zhao and Alan Seabaugh, "Low-Subthreshold-Swing Tunnel Transistors," *IEEE Electron Device Letters*, vol.27, no.4, pp. 297-300, April.2006.

[20] Shylendra Ahish, Dheeraj Sharma, Yernad Balachandra, Nitin Kumar and Moodabettu Harishchandra Vasantha, "Performance Enhancement of Novel InAs/Si Hetero Double-Gate Tunnel FET Using Gaussian Doping," *IEEE Transactions on Electron Devices*, vol.63,no.1,pp.288-295,Jan.2016. https://doi.org/10.1109/TED.2015.2503141.

[21] Rakhi Narang, Manoj Saxena, R. S. Gupta, Mirdula Gupta, "Drain current model for a gate all around (GAA) p-n-p-n tunnel FET", *Micro-electronics Journal*,44 (2013) 479-488, May. https://doi.org/10.1016/j.mejo.2013.04.002.

[22] Madan J and Chaujar R "Numerical Simulation of N + Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature," *IEEE Trans. Electron Devices*, vol.64, no.4, pp.1482–88, April 2017. https://doi.org/10.1109/TED.2017.2670603.

[23] J. Madan, R. Chaujar, Interfacial charge analysis of heterogeneous gate dielectric-gate all around-tunnel FET for improved device reliability, *IEEE Trans. Device Mater. Reliab*.16 (2016) 227-234. https://doi.org/10.1109/TDMR.2016.2564448.

[24] V. Saripalli, S. Datta, V. Narayanan, and J. P. Kulkarni, "Variation-tolerant ultra-low-power heterojunction tunnel FET SRAM design," *IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 45-52, Jun. 2011.

[25] Navlakha N, Lin JT, Kranti A, "Retention and Scalability Perspective of Sub-100-nm Double Gate Tunnel FET DRAM,"*IEEE Transactions on Electron Devices*, vol.64, no.4, pp.1561-1567, April 2017. https://doi.org/10.1109/TED.2017.2662703.

[26] G. V. Luong, S. Strangio, A. Tiedemannn, S. Lenk, S. Trellenkamp, K.Bourdelle, Q.-T.Zhao, and S.Mantl, "Experimental Demonstration of Strained Si Nanowire GAA n-TFETs and Inverter Operation with Complementary TFET Logic at Low Supply Voltages," *Solid-State Electronics*,vol.115,pp.152–159,2016. https://doi.org/10.1016/j.sse.2015.08.020.

[27] Safa S, Noor SL, Khan ZR, "Physics-Based Generalized Threshold Voltage Model of Multiple Material Gate Tunneling FET Structure," *IEEE Transactions on Electron Devices*, vol. 64, no.4, pp. 1449-1454, April 2017. https://doi.org/10.1109/TED.2017.2662580.

[28] S. Mookerjea, R. Krishnan, S. Datta, V. Narayanan, on enhanced Miller capacitance effect in interband tunnel transistors, *IEEE Elec tron Device Lett.* 30(2009) 1102-1104. https://doi.org/10.1109/LED.2009.2028907.

[29] W. Cao, C. J. Yao, G. F. Jiao, D. Huang, H. Y. Yu and M. F. Li, "Improvement in Reliability of Tunneling Field-Effect Transistor With p-n-i-n Structure," *IEEE Trans. on Electron Devices*, vol. 58, no.7,pp.2122-2126,Jul.2011. https://doi.org/10.1109/TED.2011.2144987.

[30] Pandey, Rahul, Saurabh Mookerjea, and Suman Datta, "Opportunities and Challenges of Tunnel FETs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.63, no.12, pp.2128-2138, Dec. 2016. https://doi.org/10.1109/TCSI.2016.2614698.