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Research paper

A 0.18um CMOS Low Noise Amplifier for 3-5ghz UWB Receivers

N. Malika Begum[1*], W. Yasmeen[2]

[1]M.Tech Student (VLSI & ES), Department Of ECE, G.P.R.E.C, Kurnool.
[2]Assistant Professor, Department Of E.C.E, G.P.R.E.C, Kurnool.
E-Mail:Yasmeen.W@Gmail.Com
**Corresponding Author E-Mail:Nmalikabegum@Gmail.Com*

Abstract

This paper presents an Ultra-Wideband (UWB) 3-5 GHz Low Noise Amplifier (LNA) employing Chebyshev filter. The LNA has been designed using Cadence 0.18um CMOS technology. Proposed LNA achieves a minimum noise figure of 2.2dB, power gain of 9dB.The power consumption is 6.3mW from 1.8V power supply.

Index Terms: *Ultra-wideband, low noise amplifier, chebyshev filter, noise figure.*

1. Introduction

In recent years, increasing demand for short range, wireless technology led to the development of Ultra Wideband (UWB), which is capable of transmitting data with high data rates over a wide spectrum of frequency bands. In the year 2002, Federal Communications Commission (FCC), set the standard for UWB (IEEE 802.15.3a). The UWB is spread over the frequencies of 3.1-10.6 GHz.

In UWB receivers, the Low Noise Amplifier plays a vital role, because the performance of the entire receiver is dependent on its first stage (LNA). LNA is the basic building block of the UWB receiver. Basic building block of a receiver has three stages, namely a LNA, a mixer and a filter, as shown in Fig .1. A good LNA amplifies the weak signal without adding much noise to it. A LNA is characterized by low noise figure, high gain, input and output matching. Various techniques have been proposed to implement UWB-LNA. This paper focuses on design and implementation of a UWB-LNA using Chebyshev filter in 0.18um CMOS process.

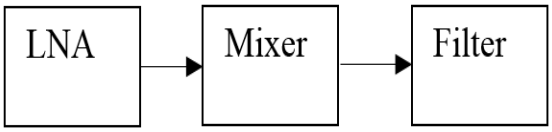

Fig. 1: Basic Building of a Receiver.

This paper is organized as follows. Section II deals with the previous work. Section III elaborates the proposed work. Section IV and Section V present results and brief conclusion respectively.

2. Previous work

Different wireless communication devices demand diverse communication standards. Instead of different amplifiers for each application, a multiband amplifier with flexibility can be designed. Numerous approaches have been proposed for implementing a UWB-LNA.

One such method is to make use of active inductor. A CMOS-LNA employing active inductor is shown in Fig.2.

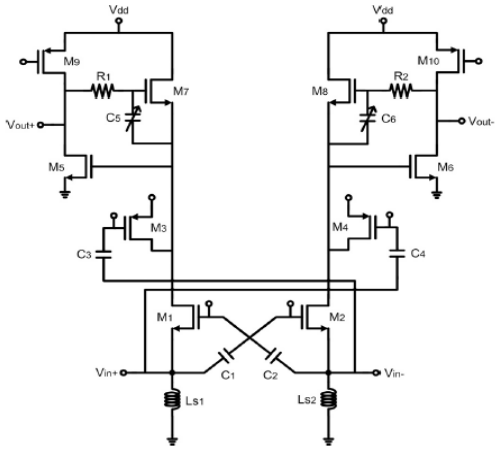

Fig.2: CMOS-LNA using active inductor.

The LNA shown in Fig.2 has three stages, namely- broadband input stage, noise cancellation stage and band selective stage. The broadband input stage is a capacitor cross-coupled differential common-gate LNA. Noise cancellation stage consists of transistors M3, M4 and these two transistors cancel the thermal noise generated by the transistors M1 and M2. Band selective stage consists of a tunable active inductor. The schematic of the LNA is shown in Fig. 3.This tunable active inductor is designed using variable capacitor. The undesired interference is attenuated by varying the value of the active inductor.

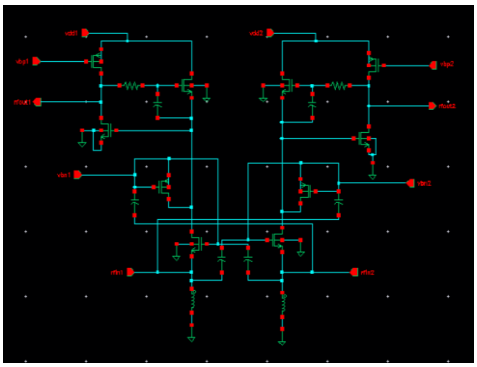

Fig.3: Schematic o the CMOS-LNA using active inductor.

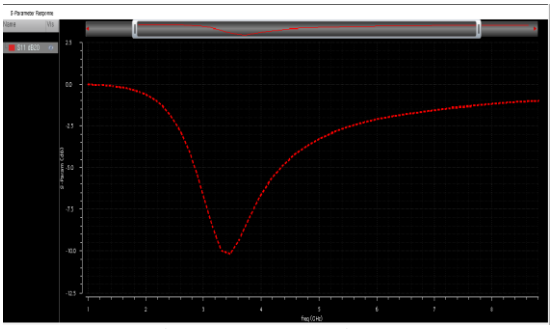

Fig. 4: Simulated frequency response of input return loss (S11).

The frequency can be shifted by tuning the effective inductance and quality factor, which is obtained by changing the bias current of the transistor M5 or M7. Fig. 4 and Fig. 5 show the simulated input and output return loss respectively.

As shown in Fig. 4 and Fig. 5, the input return loss is -10.1dB and output return loss is -10.8dB respectively. The simulated minimum noise figure is 8dB as shown in Fig. 6. The simulated gain is shown in Fig.7.

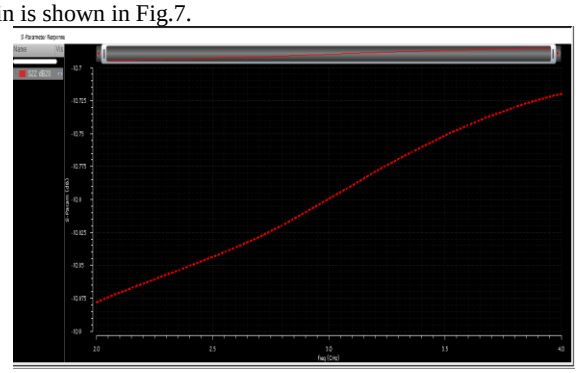

Fig. 5: Simulated frequency response of output return loss (S22).

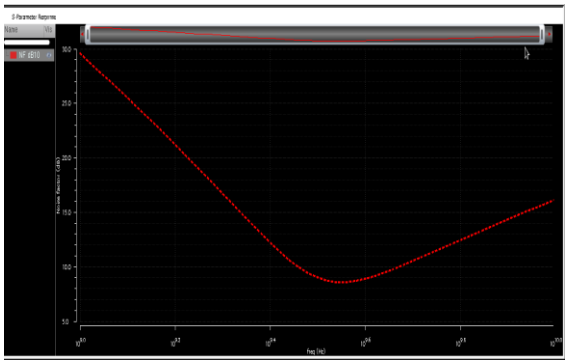

Fig. 6: Simulated NF (Noise Figure).

The LNA shown in Fig.3 has a high noise figure of 8dB, low power gain of 2dB. A LNA is desired to have a low noise figure, high gain and low return losses and it consumes 14.5mW of power from a 1.8V power supply. Moreover, LNA's employing tunable active inductors have drawbacks such as high power dissipation, non-linearity and inferior noise performance.

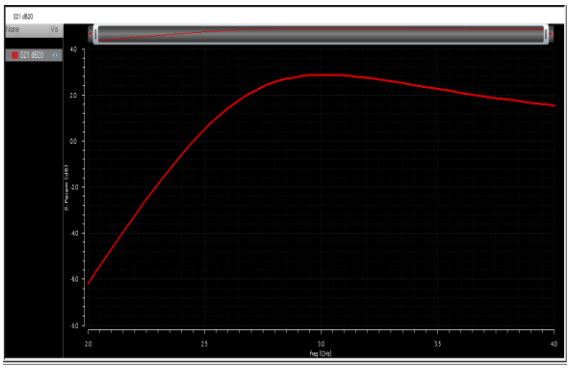

Fig. 7: Simulated power gain (S21).

This leads to designing of a LNA having low noise figure, less power dissipation, high gain. The proposed LNA, described in Section III, has the above mentioned features.

3. Proposed work

This paper presents, a Chebyshev LC band pass filter in the wideband impedance matching to interface the low noise amplifier with the antenna. The bandwidth extension of LNA can be obtained by using wideband impedance matching. The proposed LNA is shown in Fig.8.

Chebyshev filter has an advantage of sharp roll of factor in stop band and ripples in pass band. The reactive part of the input impedance over the frequency range of 3-5 GHz is resonated by the filter. Fig. 9 depicts the schematic of proposed LNA.

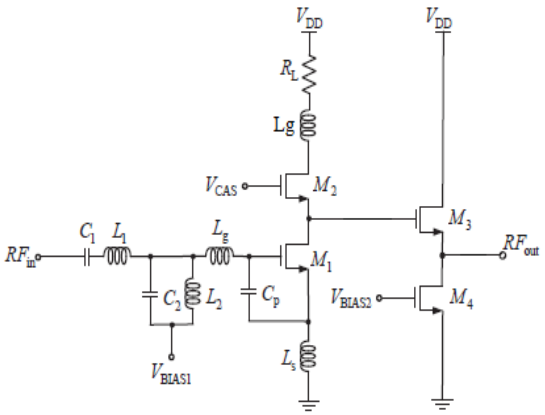

Fig. 8: Proposed LNA

As shown in Fig.8, the proposed LNA consists of a three section Chebyshev filter followed by a Cascode of common source and common gate configuration and then an output buffer, which is used only for measurement purpose. The schematic of the proposed LNA is shown in Fig. 9.

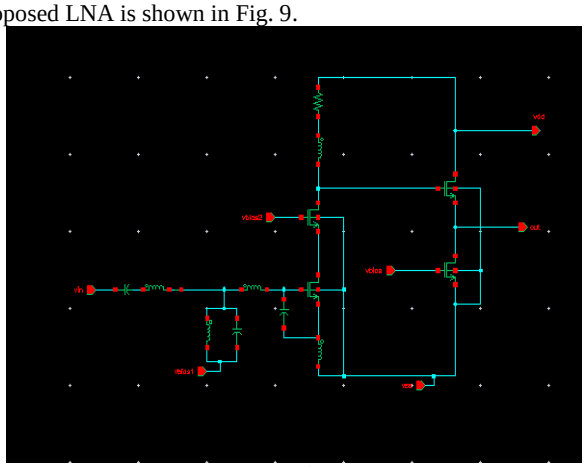

Fig. 9: Schematic of proposed LNA.

The LNA shown in Fig.8 has a series resonator (L1 and C1) at the input, followed by a parallel resonator (L2 and C2). The reactive part of the input impedance oscillates by double terminated band pass filter circuit over the frequency range of 3-5 GHz. The width of transistor M2 is optimized to a smaller value of 60um, in order to improve noise figure. The transistors M1, M2, M3, M4 have length L=0.18um. The Chebyshev filter parameters are L1, C1, L2 and C2 .The optimized component values of Chebyshev filter are 1.3 nH, 650 fF, 1.6 nH and 490 fF respectively. The width of transistors M1, M3, M4 are chosen to be 240um, 60um and 60um respectively. The source inductance Ls is set to 680 pH and Lg=1.4 nH.

4. Simulated results

S-parameters are used to measure the performance of LNA in terms of gain, noise figure, return losses. The simulated input and output return losses of the proposed LNA are shown in Fig. 10 and Fig. 11 respectively.

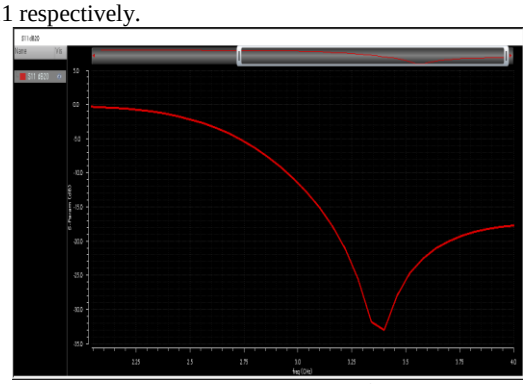

Fig. 10: Simulated input return loss (S11) of the proposed LNA.

The simulation results show that input return loss is -32dB and output return loss is -10dB.The power gain, noise figure of the proposed LNA are shown in Fig. 12 and Fig. 13 respectively.

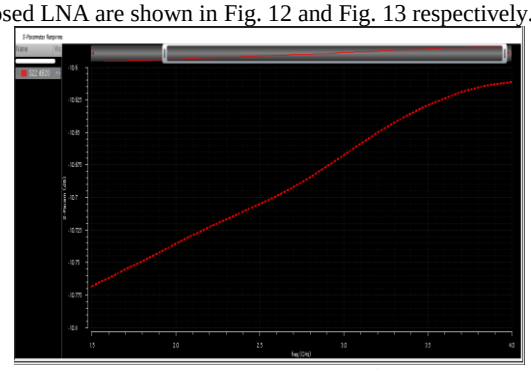

Fig. 11: Simulated output return loss (S22) of the proposed LNA.

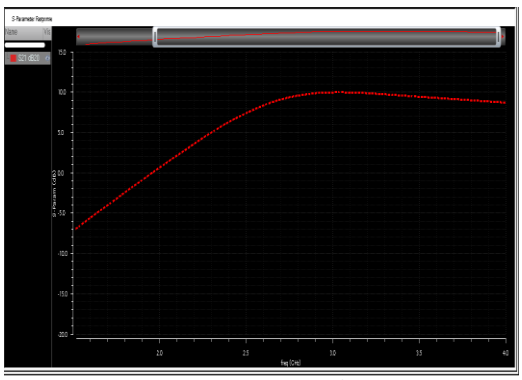

Fig. 12: Simulated power gain (S21) of the proposed LNA.

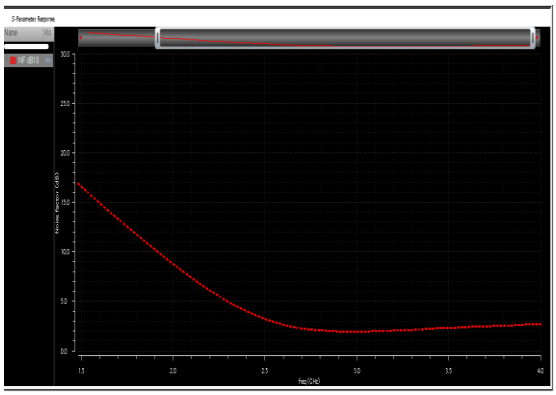

Fig. 13: Simulated noise figure (NF) of the proposed LNA.

The parameters of the previous and proposed work are listed in Table-I.

Table-I

Parameters	Previous work	Proposed work
Technology	CMOS 0.18um	CMOS 0.18um
Supply Voltage	1.8	1.8
Frequency (GHz)	3-5	3-5
S11 (dB)	-10.1	-32
S21 (dB)	2	9.5
S22 (dB)	-10	-10.6
Noise Figure	8.6	2.2

5. Conclusion

The LNA using 0.18um CMOS technology is designed for 3-5 GHz, using a Chebyshev filter. The designed LNA achieves low noise figure, low return losses. In general, the desired gain of LNA should be above 10dB. Despite having a gain of 9.5dB, the simulated results of the proposed LNA, show high performance with low power consumption.

References

[1] Zulkepli SNIS & Zulkifli TZA, "Asymmetric T-coil, resistive feedback Cascode low noise amplifier for ultra-wideband receiver", *IEEE International Circuits and Systems Symposium (ICSyS)*, (2015), pp. 11-16.

[2] Shim J, Yang T & Jeong J, "Design of low power CMOS ultra wide band low noiseamplifier using noise canceling technique", *Microelectronics. J.* Vol.44, No.9, (2013), pp.821–826.

[3] Zhao Y, Zhang W, Xie H, Gao D & Fu Q, "An improved active inductor with tunable active resistor feedback and multi-regulated cascode circuit", *Sens. Transducers*, Vol.172, No.6, (2014), pp.191–195.

[4] Kia HB, A'ain AK, Grout I & Kamisian I, "A reconfigurable low-noise amplifier using a tunable active inductor for multistandard receivers", *Circuits, Syst., Signal Process*., Vol.32, No.3, (2013), pp.979–992.

[5] Hashemi H & Hajimiri A, "Concurrent multiband low- noise amplifiers theory, design, and applications", *IEEE Trans. Microwave Theory Tech.*, Vol.50, (2002), pp.288-301.

[6] Slimane A, Taibi A, Saadi AA, Maafri D, Tedjini S & Traiche S, "A power constrained simultaneous noise and input matched low noise amplifier design technique", *IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS)*, (2016), pp.1-4.

[7] Meaamar A, Boon CC, Do MA & Yeo KS, "A Wideband Low Power Low-Noise Amplifier in CMOS Technology", *IEEE Trans. Circuits Syst.*, Vol.57, (2010), pp.773-782.

[8] Kim CW, Kang MS, Anh PT, Kim HT & Lee SG, "An ultra-wideband CMOS low noise amplifier for 3-5 GHz UWB system", *IEEE J. Solid-State Circuits*, Vol.40, (2005), pp.544-547.