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Research paper

Design of ASIC Square Calculator Using AncientVedic Mathematics

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Abstract

This article includes a simple design of Vedic square calculator for Application Specific Integrated Circuit (ASIC). This is a straightforward and innovative design of Vedic calculator using only few basic digital logic gates. Among the all sutras and sub sutras of ancient Vedic mathematics, the sutra 'Urdhva Tiryagbyham' is used here for square calculation of two bits numbers which results in an effortless and faster method of square calculation than all the existing methods. The design and minimization of the circuit has been carried out to achieve a standard architecture that is the simplest too. Here Xilinx ISE software tool is used rigorously to simulate the architecture.

Keywords: *Multiplier; Square calculator; Urdhva Tiryagbyham; Vedic mathematics.*

1. Introduction

Multiplication is a basic mathematical operation for all processors. The squaring means self multiplication, i.e. multiplicand and multiplier are same. Lots of popular Vedic multipliers with verities of advantages and disadvantages are available and fascinated the interest of researchers. Thus designing a self multiplier or square calculator or squarer is of course a noteworthy attempt. In this article the ancient Vedic mathematics formula is used purposefully for the enhancement of calculation speed.

Many popular existing multipliers are there for different applications, like the digital processor's multipliers, named DSP multiplier [1]. A reduced bit UT-multiplier proposed in 2008 [2]. The array multiplier and UT-multiplier up to four bits discussed earlier [3]. A good approach of 64 bits squarer is projected already [4]. In 1951, the multiplication method of signed binary numbers has been discussed [5]. 32 bits multiplier for faster operation has been considered previously [6]. In 2004 the architecture of Overlay multiplier has already been taken care of [8]. EDA tool multiplier is also there in research of multipliers [9]. Several hardware implementations of different multipliers using Vedic concepts have also been anticipated. Area efficient NND multiplier using Vedic sutras have been implemented [10]. A comparison of hardware based conventional multipliers vs. Vedic multipliers is done [11]. A 32×32 bits multiplier and it's hardware implementation is done formerly [12]. Factorial calculator is also implemented earlier [13]. The matrix multiplier has already haggard the attention of the experimenter [14]. The multiplier model to multiply special numbers is also noteworthy here [15-16]. But among all discussed multipliers, the recent ASIC square calculator is well accepted [17].

A new modified architecture of recently proposed multiplier [17], which is the simplest and minimized one for square calculation, is designed here for Application Specific Integrated Circuit (ASIC). But the design proposed here includes only a few number of fundamental digital logic gates by successfully applying the concept of Vedic formula. In all probability this type of Vedic square calculator has not been implemented before. Popular ISE Xilinx software tool has been used for the confirmation of the proposed architecture.

2. Vedic Mathematics

Swami Bharati Krishna Tirtha (1884-1960), former Jagadguru Shankarachraya Maharaj selected a set of sixteen Sutras and thirteen Sub Sutras from 'Atharva Veda' [7]. Vedic mathematics is an 'Upa Veda' of 'Atharva Veda'. Vedic mathematics is advantageous in reducing the complexity of conventional methods and turns into simpler calculation technique. As the formulas and sub formulas resembles very closely the human brain functions, this is a very appealing field, not only for mathematicians but also for engineers [5]. The sutra 'Urdhva Tiryagbyham' ('UT') is used here to implement the proposed squarer. The sutra means 'vertically and crosswise' operations. Calculations become simpler by applying this formula in multiplication techniques [7]. The multiplication method using 'UT' sutra leads to lesser steps, space, and further reduces the calculation burden. The sutra has been efficiently used in this article.

3. Proposed Design

Two bits multiplier and two bits multiplicand numbers are multiplied here. The procedure of multiplication is discussed below.
At first the least significant bits (LSBs) are multiplied (vertical) i.e. both the LSBs of multiplier and multiplicand is multiplied first to get least significant bit (LSB) of the resultant product.

Second step is crosswise multiplication. The product of multiplicand's LSB bit to the multiplier's MSB bit is added up with the product of multiplicand's MSB bit to multiplier's LSB bit. This results second bit of the ensuing product and the generated carry in this step is forwarded to add in the output of next stage. In last step, it is again vertical. The multiplication of multiplier-multiplicand's MSBs is done here. The result of this step is added with earlier step generated carry. This is the multiplication procedure for two bits numbers using the formula 'Urdhva Tiryagbyham'.

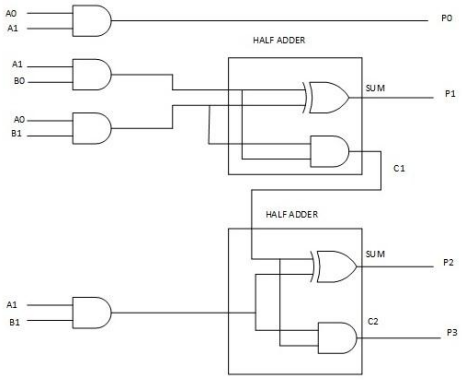

Fig. 1: Main Vedic multiplier

The parent circuit of multiplication using the above discussed method is shown in Fig. 1. Here multiplicand is A= A0A1 (two bits) and multiplier is B= B0B1 (two bits). The output P= P0P1P2P3 is four bits where carry C1 is coming from second step and carry (C2) in last step is the MSB of sum (P3).

The plan of Vedic calculator using the above described technique is proposed recently [17] and the architecture is shown in Fig. 2. Here two bits multiplicand is X= X0X1 and in parallel two bits multiplier is X= X0X1 as it is square calculator, hence self multiplier. Therefore the multiplier and multiplicand both are same (A= B =X).

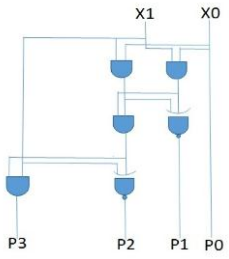

Fig. 2: Recently proposed [17] architecture

The proposed ASIC Vedic calculator is the modified and minimized version of the above discussed architecture. The projected design (as shown in Fig. 3) contains of only two XOR gates and one AND gate unlike the recently proposed [17] squarer where two AND gates and two Half adders are used. Here the input is X= X0X1 (two bits) and the result is P= P0P1P2P3 (four bits).

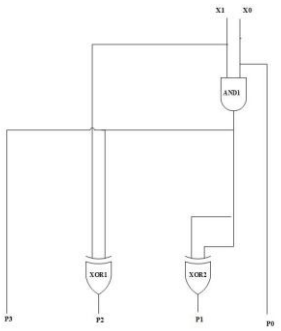

Fig. 3: Proposed architecture

4. Simulation Results

The output of proposed squarer or square-calculator has been tested fruitfully in Xilinx 14.1 Integrated Software Environment. The top module of proposed squarer in Xilinx ISE is shown in Fig. 4, where input is X= X0X1 and result is P= P0P1P2P3.The RTL schematic in this regard is shown in Fig. 5. The simulation report and the project status report of the squarer are exposed in Fig. 6 and Fig. 7 respectively. Fig. 8 is the snap-shot of device utilization summary of the simulation process which guaranteed the successful simulation of the calculator with no errors and warnings.

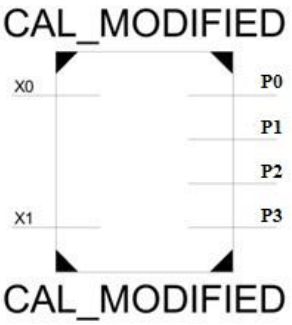

Fig. 4: Top module of proposed calculator

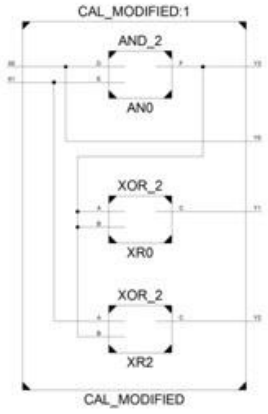

Fig. 5: RTL schematic of proposed calculator

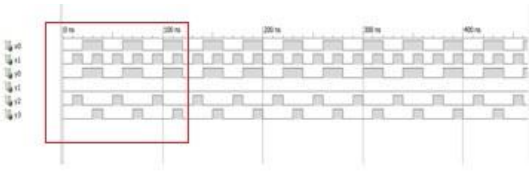

Fig. 6: Simulation report of proposed calculator

CAL_MODIFIED Project Status (03/25/2017 - 10:01:49)			
Project File:	CALC_MODIFIED.xise	Parser Errors:	No Errors
Module Name:	CAL_MODIFIED	Implementation State:	Synthesized
Target Device:	xc3s500e-4fg320	• Errors:	No Errors
Product Version:	ISE 14.1	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Fig. 7: Project status report of proposed calculator

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	1	4656	0%
Number of 4 input LUTs	2	9312	0%
Number of bonded IOBs	6	232	2%

Fig. 8: Device utilization summary

5. Comparisons

The projected Vedic square calculator has been designed here and it has been simulated successfully. With analysing the simulation report and device utilization summary of the proposed squarer, it has been compared to the popular already proposed [17] architecture as shown in TABLE I. The performance of the projected improved design exactly same as its main architecture [17], but advantage is that the area usage is very lesser as only 3 digital gates are sufficient to complete the design instead of 6 gates.

Table 1: Comparison table

Parameters	Square Calculator	
	Previously proposed [17]	Proposed in this paper
No. of gates	6	3
No. of occupied slices	Used/Available	Used/Available
	1/4656	1/4656
No. of 4 input LUTs	Used/Available	Used/Available
	2/9312	2/9312
No. of bonded IOBs	Used/Available	Used/Available
	6/232	6/232

6. Conclusion and Future Extent

The architecture of square calculator, the simulation, and comparison with existing recently proposed architecture [17] has been presented effectively. This circuit has lesser complexity and it occupies a smaller area compared to the existing multipliers, and in addition this is probably the simplest Vedic squarer till now.
However, this work can be expanded for 'n' bits squarer instead of merely two bits and may be implemented in FPGA kits also for hardware implementation.

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