International Journal of Engineering &Technology, 7 (3.12) (2018) 232-234

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

A Study on Electrical Characterization of Surface Potential and Threshold Voltage for Nano Scale FDSOI MOSFET

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Abstract

In this paper the study of electrical characterization of Surface potential & Vth threshold-voltage model is developed for FD SOI MOSFET. The threshold voltage is important parameter in device design. Scaling of device has positive impact on device performance. The various parameters like thickness of silicon film, oxide layer, drain to source voltage plays a key role in improvement of device performance. Surface potential explain the distribution of applied potential throughout the channel. We also analyzed the effect of threshold voltage with various electrical parameters.

Keywords: *Nano scale, Short-channel effects, silicon- on-insulator (SOI), channel length, 3-D, surface potential, MOSFET, Threshold voltage.*

1. Introduction

Complementary Metal oxide semiconductor has been a radical invention in Very large scale industry field and serves as the main component of every electronics device (like mobile, computer, etc.) right from its inception [1-4]. For faster, cheaper and smaller size devices, it has been there in the eyes of researchers to trim down the device size below sub 50nm levels. But as the device minifies, the concern that arises is the degradation of the device performance with gradual decrease in channel length which are collectively called the SCEs [4]. This brings the new technology in play called the SOI [5]. The SOI technology is widely used in the semiconductor devices between channel and substrate. The SOI MOSFETs performance increases due to various reasons like reduced parasitic capacitances. The SOI MOSFETs are more advantageous in comparison to conventional due to no floating body effect present in device. The low leakage effect free from kink effect make the SOI devices more effective in comparison to conventional MOSFETs [11-13]. The channel of SOI MOSFET further classified as fully and partially depleted. In a Fully Depleted Silicon on Insulator Metal Oxide
Semiconductor Field Effect Transistor the Si substrate being very thin is fully depleted eliminating any floating body effect. The front and back gates (bulk Si below the insulator can be viewed as the second gate) are electro statically coupled. Unlike PDSOI, Ψ_{SF} is a function of Ψ_{SB}. Only the valence and conduction band edges are shown for simplicity. The Fully Depleted Silicon on Insulator is advantageous over partially depleted SOI MOSFET in terms of FD circuits are having low noise, very easy to design, floating body effect is low, kink effect is low as compared to PD circuits to suppress the effect of Scaling, which is responsible for device performance degradation.

Due to continuous minimization of physical device dimensions the conventional MOSFETs are stuck at performance aspects [9-10]. The SOI MOSFETs are different from conventional MOSFET in structural difference i.e. a layer of SiO_2 is introduced.

2. SOI MOSFET Device Structure

In comparison to conventional MOSFET, SOI MOSFET uses silicon insulator silicon substrate. On the basis of thickness of SOI (Silicon on Insulator) layer the MOSFET further categorized as Fully Depleted and Partially Depleted MOSFETS [7]. In partially Depleted SOI MOSFETs the thickness of insulator layer is kept more in comparison to depletion width of gate (50-100 nm).The main advantage over the conventional MOSFET are operated at low power, performance gain of 18-35%.In Fully Depleted SOI MOSFET as shown in figure[1] the channel is completely depleted via majority carriers as the silicon layer is thin (5-25nm).The advantage of fully depleted over partially depleted is to eliminate the floating point effect. Difference between FDSOI MOSFET and PDSOI MOSFETs has been shown in table 1(8).SOI MOSFET is also better than bulk-Si as it reduced the parasitic capacitance, short channel effects and can be used for simplifying the process.

Table 1: Difference between FDSOI MOSFET and PDSOI MOSFET

FDSOI MOSFET	**PDSOI MOSFET**
Thickness of Insulating BOX is 10-50 nm	Thickness of Insulating BOX is 90-200 nm
Top Silicon layer is 5-25nm	Top Silicon layer is 50-100 nm
It is used in low power application	It is used in analog circuits
Easy to design	Complex to design

3. Device Modeling

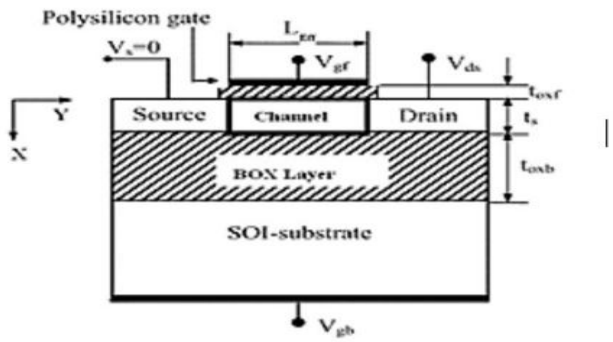

Fig. 1: Cross Section View (x-y) of FDSOI MOSFET

$$\frac{\partial^2 \phi(xyz)}{\partial x^2}+\frac{\partial^2 \phi(xyz)}{\partial y^2}+\frac{\partial^2 \phi(xyz)}{\partial z^2} \quad (1)$$

The 3D Poisson's equation for Fully Depleted SOI MOSFET can be given by the equation[9] Here N_A represents the doping concentration and $\phi(x,y,z)$ is the surface potential at point(x,y,z).The solution of Possion's equation with required boundary conditions [6]are given below as

$$\phi(0,y,z)-\frac{t_{oxf}}{\epsilon_{ox}}[\epsilon_{si}\frac{\partial\phi(x,y,z)}{\partial x}|_{x=0-}Q_{it}{}^{f}]=V_{gf}-V^{f}{}_{fb} \quad (2)$$

$$\phi(t_{si},y,z)-\frac{t_{oxf}}{\epsilon_{ox}}[\epsilon_{si}\frac{\partial\phi(x,y,z)}{\partial x}|_{x=tsi+}Q^{b}{}_{it}=V_{gf-}V^{b}{}_{fb}) \quad (3)$$

$$\phi(x,0,z)=V_{bi} \quad (4)$$

$$\phi(x,L_{EFF},Z)=V_{bi}+V_{ds} \quad (5)$$

$$\phi(x,y,0)-\frac{t_{oxw}}{\epsilon_{ox}}[\epsilon_{si}\frac{\partial\phi(x,y,z)}{\partial x}|_{z=0-}Q_{it}{}^{f}]=V_{gf}-V^{f}{}_{fb} \quad (6)$$

$$\phi(x,y,w)+\frac{t_{oxw}}{\epsilon_{ox}}[\epsilon_{si}\frac{\partial\phi(x,y,z)}{\partial x}|_{z=w+}Q_{it}{}^{f}]=V_{gf}-V^{f}{}_{fb} \quad (7)$$

$$\frac{d^2\phi l(x)}{dx^2}=\frac{qN_Ax}{\epsilon_{si}} \quad (8)$$

$$\frac{d^2\phi\prime(x,y)}{dx^2}+\frac{d^2\phi\prime(x,y)}{dy^2}=0 \quad (9)$$

$$\frac{d^2\phi"(x,y,z)}{dx^2}+\frac{d^2\phi"(x,y,z)}{dy^2}+\frac{d^2\phi"(x,y,z)}{dy^2}=0 \quad (10)$$

4. Result and Discussion

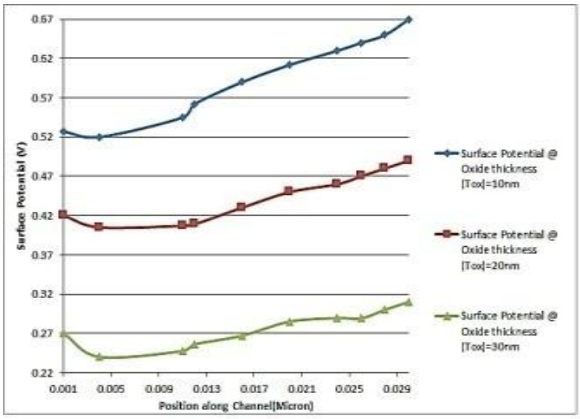

Fig. 2: Channel potential variation with normalized positionalong the channel length at Vds 0.5 V

From figure The distribution of Surface potential inside the channel is represented at particular thickness of silicon layer,the distribution of surface potential also varies from source to drain terminals.The minimum surface potential is observed in the region near to source terminal and maximum potential is observed in the region towards drain terminal.

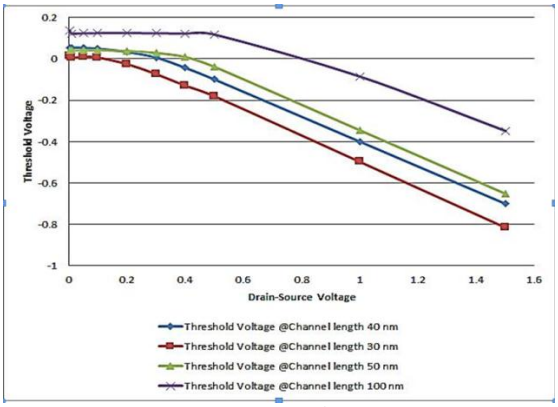

Fig. 3: Threshold Voltage variation for varying channel length

Figure describes the variations in threshold voltage with channel length along with V_{ds}, drain to source voltage, As we reduced the length of the channel , threshold voltages vary accordingly due to the electrons now require less distance.

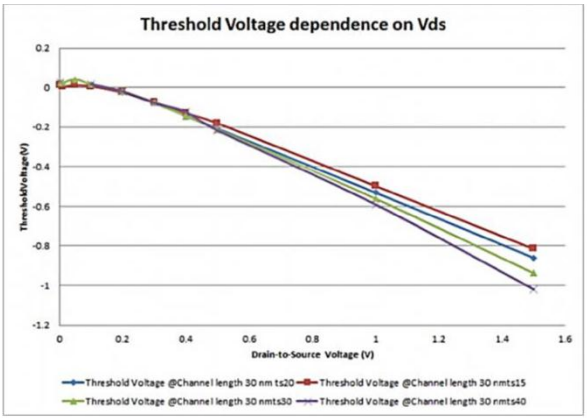

Fig. 4: Threshold Voltage Dependence on thickness of Si film for effective channel length 30nm and t_s 15,20,30,40 nm

Figure describes the variations in threshold voltage with thickness of silicon layer along with V_{ds}, drain to source voltage, As we reduced the thickness of silicon layer , threshold voltages vary accordingly due to the increse in controlabilty of electron in channel and further reduced as drain to source to voltage increased.

5. Conclusion

The effect of threshold voltage is prominent in increase of device performance. The length of the channel is another parameter which can be utilized to enhance the performance of the SOI MOSFET in nano scale range. The physical dimension of the device shrinks micrometer to nano meter and the device performance enhanced. In case of 100 nm , 50nm, 40nm,30nm channel length devices the device performance increased in terms of better threshold voltage of the SOI devices which is essential for low power consumption issues.

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