International Journal of Engineering & Technology, 7 (3.27) (2018) 531-534

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Type-2 Fuzzy Logic Controlled Adjustable Step-Size LMS Algorithm for DSTATCOM

Ganji Vivekanand [1], Dr.K. Chandra sekhar[2], D. Suresh[3]

[1]*Research Scholar, Acharya Nagarjuna university, Guntur*
[2]*Prof & Head, Dept of EEE., RVR&JC Engineering college, Guntur*
[3]*Vignan college of Engineering & Technology*

***Abstract*:**

In this paper, voltage source converter is utilized as a distributed static compensator (DSTATCOM). The voltage source converter has advantages of lower capacitor size and reduced switching losses. The DSTATCOM is used to elimination of harmonics and reactive power of the nonlinear load. The reference currents of DSTATCOM estimated with type-2 fuzzy logic control step-size updated least mean square algorithm.

Conventionally, the proportional integral controller is used for control of dc link voltage and current of DSTATCOM. The proportional controller requires in detailed mathematical modeling of the overall system and it is tedious process. To overcome aforementioned task interval type-2 fuzzy logic controller (IT2FLC) applied for a voltage source converter based DSTATCOM. The proposed IT2FLC is utilized to regulate the DC voltage as well as update the step size of the algorithm to improve the performances of the DSTATCOM. The overall system of DSTATCOM including T2FLC implemented in MATLAB/Simulink. The simulated response of DSTATCOM found to be improved and better than the conventional LMS algorithm controller.

Keywords:-*type-2 fuzzy logic controller, DSTATCOM*

1. Introduction

The large amount of world energy is processed through power electronics equipment such as variable-frequency drives, computers and electronic ballasts and so on. These heaps contribute the colossal sounds to the utility which are odd different of the principal frequency. The harmonics cannot contribute the active power and hence, need to be compensated. To dispose of the music, dynamic power filter has been proposed. The active filter is called as DSTATCOM [1]-[5].

The most of the DSTATCOMs are based on shunt coupled active power filter, which is used for compensation of harmonics and volatile power of the nonlinear load. The family of DSTATCOMs referred with single name that is custom power devices. The custom power devices are DSTATCOM, dynamic voltage restorer and compensator of integrated power quality etc. The DSTATCOM is multifunctional device which provide the harmonics elimination, reactive power compensation, voltage regulation, power factor correction, load balancing and termination of the line.

The execution of the DSTATCOM to a great extent relies upon the ongoing estimation of the remuneration current. The most usually utilized strategies in literature are instantaneous and synchronous theory-based detection of the compensation current. Because of its ease of calculation of harmonics currents and self learning ability, adaptive control scheme gain attention in the estimation of reference currents [13]. In this paper, LMS algorithm with T2FLC used for step size adjustment is arrived for harmonics current estimation. The T2FLC along with average estimation is used for updating of the step-size of the least mean square algorithm. The dc link also regulated with type-2 fuzzy logic controller.

The controller design is the major part of the DSTATCOM for proper tracking the desired response. Conventionally controller of PI is utilized for regulating voltage of the DC link of DSTATCOM. However, the parametric value of PI controller requires rigorous mathematic modeling of the system, which is very difficult to obtain parameter of PI controller under uncertainty condition and external load disturbance etc. [5].

In recent times, IT2FLC generated great deal of interest in most of control system applications. The advantages of the fuzzy logic controller against the PI controller is that the overall modeling and computation of parameter is not require and also handle imprecise input and so on.

In this paper, IT2FLC based variable step size is proposed for elimination of harmonics and reactive for DSTATCOM. A control theory based on T2FLC used is for step-size updating of LMS algorithm and also dc link connects voltage regulation of DSTATCOM. The execution of DSTATCOM with with IT2FLC is evaluated through computer MATLAB simulation study.

2. Configuration of DSTATCOM Topology

The configuration of the power system with DSTATCOM is shown in Fig.1. The six-pulse diode bridge rectifier used as a nonlinear load to test The execution of DSTATCOM. The DSTATCOM based on voltage source inverter is realized using 6 insulated gate bipolar transistors (IGBT), three inductors and six dc capacitors. The DSTATCOM constructed on voltage source inverter is connected to PCC through interfacing inductors.

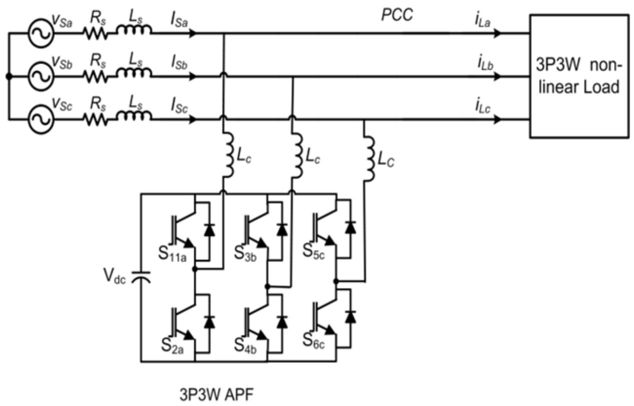

Fig. 1: Topology of DSTATCOM.

3. Control Scheme of DSTATCOM

The current tracking capability of an active power filter depends on its compensation current estimation. The instantaneous source voltage is

$$v_{s_h}(t)=V_{m_h}\sin(\omega t) \tag{1}$$

When the load is coupled to the source, which is highly nonlinear cause more harmonics pollution to the source. The nonlinear current of the load is integer multiple of third harmonics current, which can be given as follows:

$$\begin{aligned} i_{L_h}(t) &= \sum_{n=1}^{\infty} I_{n_h}\sin\left(n_h\omega t+\phi_{n_h}\right) \\ &= I_{1_h}\sin\left(\omega t+\phi_{1_h}\right) \\ &+\sum_{n_h=2}^{\infty} I_{n_h}\sin\left(n_h\omega t+\phi_{n_h}\right) \end{aligned} \tag{2}$$

Thus, the instantaneous load current further expressed as:

$$\begin{aligned} i_{L_h}(t) &= I_{1_h}\sin(\omega t)*\cos\left(\phi_{1_h}\right) \\ &+I_{1_h}\sin\left(\phi_{1_h}\right)*\cos(\omega t) \\ &+\sum_{n=2}^{\infty} I_{n_h}\sin\left(n_h\omega t+\phi_{n_h}\right) \end{aligned} \tag{3}$$

The load current is modelled as:

$$i_{L_h}(t)=i_{f_h}(t)+i_{r_h}(t)+i_{h_h}(t) \tag{4}$$

$$i_{L_h}(t)=i_{f_h}(t)+i_{c_h}(t) \tag{5}$$

The estimated reference current is the totality of the reactive and harmonics current. The remunerating current infused by dynamic power channel is

$$\begin{aligned} i_{c_h}(t) &= i_{L_h}(t)-i_{f_h}(t) \\ &= i_{L_h}(t)-I_{1_h}\cos(\phi)\sin(\omega t) \end{aligned} \tag{6}$$

From (6), after compensation with DCMLI filter, the current drawn by the source is

Where $I_m = I_1\cos\phi_{1_h}$

$$i_{c_h}(t)=i_{L_h}(t)-I_{m_h}\sin(\omega t) \tag{7}$$

$$i_{c_h}(t)=i_{L_h}(t)-W_{A_h}\sin(\omega t) \tag{8}$$

According to the least square algorithm, the weight updates can be given as

$$\begin{aligned} W_{A_C}(n+1) &= W_{A_C}(n)+ri_c(n)\sin(\omega t) \\ W_{B_C}(n+1) &= W_{B_C}(n)+ri_c(n)\sin\left(\omega t-\frac{2\pi}{3}\right) \\ W_{C_C}(n+1) &= W_{C_C}(n)+ri_c(n)\sin\left(\omega t-\frac{4\pi}{3}\right) \end{aligned} \tag{9}$$

Where, *r* is the learning rate. The value of convergence rate is from 0.1 to 1.0. The control strategy for derived equation (9) is given in Fig.2.

4. T2FLC Based Adjustable Step-Size LMS Algorithm

The schematic outline for LMS calculation with T2FLC is appeared in Fig.2. Reference remunerating currents calculated in equation (9) are used for updating the step size of LMS algorithm. The remunerating current and rate of progress of blunder processed through type-2 fuzzy logic controller.

The load current noise signal and also the system signal to noise ratio also low the noise. The normal estimation of mistake flag is utilized to control the refreshing of the step-size of the algorithm. The estimator in light of normal estimation of mistake is

$$p(n)=\left[(\psi-1)\,p(n-1)+e(n)\right]/\psi \tag{10}$$

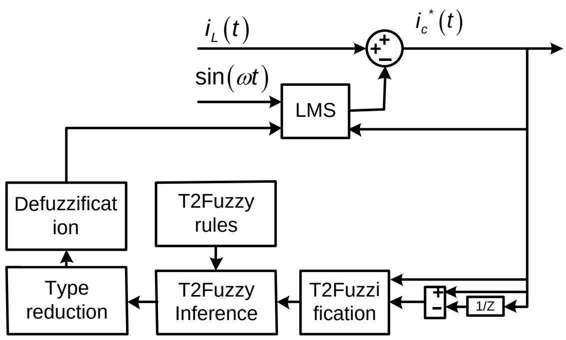

Fig. 2:. T2FLC based adjustable step-size LMS algorithm.

Where $(\psi>1)$ is utilized to modify the impact of load current signal to the system. The above formula (10) is used to keep the error signal and average data within the window. It can reduce irrelevant noise signal and zero-mean white-noise signal as well. The estimated reference current used for harmonics detection and decrease of whole harmonics in the feedback signal e(n).
the fuzzy inference for updating of the step-size is as follows.

$$\Delta r = T2FIS\left[p(n)\right] \tag{11}$$

WhereT2FIS is the type-2 fuzzy inference functions mechanism. To get the increment in the step-size Δr through the type-2 fuzzy inference mechanism and formula used for it is as follows

$$r(n+1) = r(n) + ksign\left[\Delta e(n)^2\right]\Delta r \quad (12)$$

$$\Delta e(n)^2 = e(n)^2 - e(n-1)^2 \quad (13)$$

Where k is constant and utilized to alter the difference in step-size of variable step-size LMS algorithm. To ensure the stability of the e LMS algorithm, the range of step-size r is limited.

$$r_{\min} < r < r_{\max} \quad (14)$$

The selection of $r_{\max}$ should ensure the stability of the algorithm; the selection of $r_{\min}$ should take into account the convergence speed and steady-state offset. The fuzzy rule used for step size adjustment is shown in the Table I.

Table 1: Fuzzy inference

$p(n)$	Δr
T2S	T2S
T2M	T2M
T2L	T2L

5. Interval Type-2 Fuzzy Logic Controller

The Fuzzy sets are used to epitomise vagueness and uncertainty of linguistic problems mathematically. Fuzzy logic is form of logic, which manages estimated as opposed to exact mode of reasoning. Most of the controller is based on fuzzy type-1 controller for control system applications. However, the type-1 fuzzy controllers have difficult in modelling and limiting the impact of uncertainty. One the limiting the ability of type-1 fuzzy logic is its membership function (MF) which handles uncertainty and takes crisp value as input. Recently, type-2 fuzzy set introduced, which deal with a fuzzy-fuzzy set where the grade of membership is type-1 fuzzy sets rather than the crisp value as input.
Fig. 3 illustrates the type-2 fuzzy MF, which can be achieved with type-1 fuzzy membership by blurring it. The shaded area represents the level of uncertainty and also called foot point of uncertainty (FOU). The zone amongst upper and lower enrolment MFs represents the level of uncertainty handle by T2FLC. Therefore, it is effective in handling the vulnerabilities related with process [10]

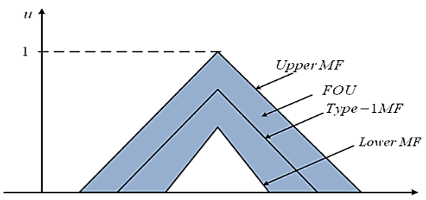

Fig. 3: Type-2 fuzzy sets.

6. DC voltage regulator

The voltage of dc link of the DSTATCOM converters implemented with IT2FLC. The IT2FLC based controlled outer voltage regulator loop is shown in Fig. 4. The inputs to the T2FLC are error e_n and change in error with respect to time ce_n

$$e_{nA}(n) = \Delta v_{dc_A}(n) = v^*_{dc_A}(n) - v_{dc_A}(n) \quad (15)$$

$$ce_A(n) = \Delta v_{dc}(n) = v^*_{dc_A}(n) - v_{dc_A}(n-1) \quad (16)$$

The output of IT2FLC is the change in loss component of active power. The output of T2FLC at nth and (n-1)th sampling instants are $i_{d_A}(n)$ and $i_{d_A}(n-1)$ respectively. The total output active power at nth sampling is determined by adding the previous value of active loss component of power with current value to the calculated change in loss power component.

$$i_{d_v}(n) = i_{d_v}(n-1) + \delta i_{d_v}(n) \quad (17)$$

Where n is the sampling time, i_{d_v} is the active loss power of desired reference active power at nth sampling time and δ is gain factor of the T2FLCs. The rule base of the T2FLC is shown in Table II. The voltage regulator loop for phase-a is exposed in Fig. 6. The rue base table T2FLC is shown Table I.

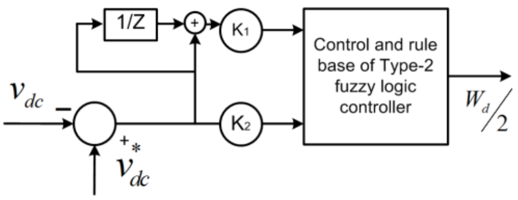

Fig. 4: T2FLC based voltage regulator.

Table II: Fuzzy logic rule base

E/CE	ANL	ANM	ANS	AZE	APS	APM	APL
ANL	ANL	NL	ANL	ANL	ANM	ANS	AZE
ANM	ANL	AFNL	AFNL	ANM	ANS	AZE	APS
ANS	ANL	ANL	ANM	ANS	AZE	APS	APM
AZE	ANL	ANM	ANS	AZE	APS	APM	APL
APS	ANM	ANS	AZE	APS	APM	APL	APL
APM	ANS	AZE	APS	APM	APL	APL	APL
APL	ANL	ANM	ANS	AZE	APS	APM	APL

7. Simulation Results

The simulated response of the DSTATCOM is presented to validate the T2FLC controller for the A DSTATCOM. The simulated response of the DSTATCOM with controller of PI is shown in Fig. 5. Before compensation with DSTATCOM, the current of the source comprises multiple of triple harmonics and reactive component of current. The source current total harmonics distortion before compensation found to be 26.76%. At instant t=0.05sec., when DSTATCOM switched-on source current tend to sinusoidal waveform and in synchronous with source voltage waveform. At same instant, the DSTATCOM voltage gradually increases and settled down at reference value. The settling period obligatory for the voltage to reach reference value is 0.1 sec. the total harmonics distortion source current after compensation with DSTATCOM is 2.13%.

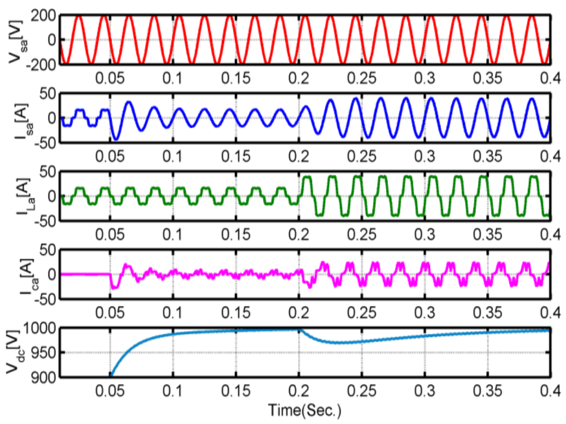

Fig. 5. Simulated waveform with PI controller.

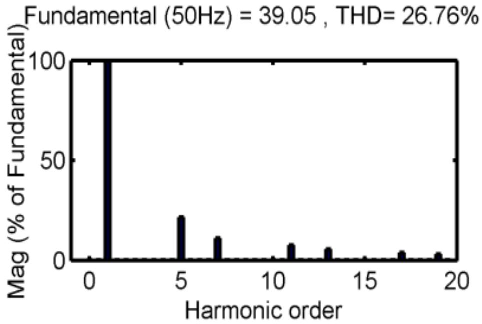

Fig. 6:. Source current THD without compensation

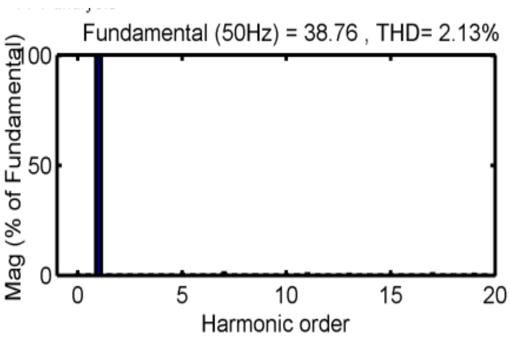

Fig. 7. The current of the source THD with compensation. With the step change in the load current, the corresponding changes in load current and compensating current observed. The changes in source current and compensating current restored within 4-6 cycles**.**

The current and voltage waveforms of DSTATCOM with T2FLC is shown in Fig. 8. Before compensation with DSTATCOM source current is non-sinusoidal waveforms and shape of waveform in stepped form. When DSTATCOM switched-on at t=0.05sec., the source current is in sinusoidal shape and in phase with source voltage waveform. The source current total harmonics distortion found to be 2.13%. This is within the recommend standard of IEEE standard. The voltage of dc link waveform is depicted in Fig.8. The voltage of dc link gradually increases, when DSTATCOM is connected at t=0.05 sec., and reaches to steady at t=0.05sec. It is evident from the simulation results the dynamics performance of DSTATCOM is better than the

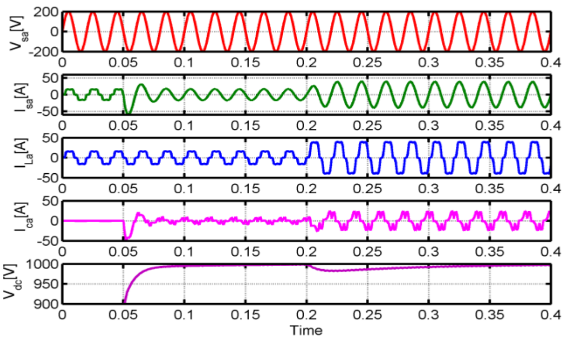

Fig. 8:. Simulated waveform

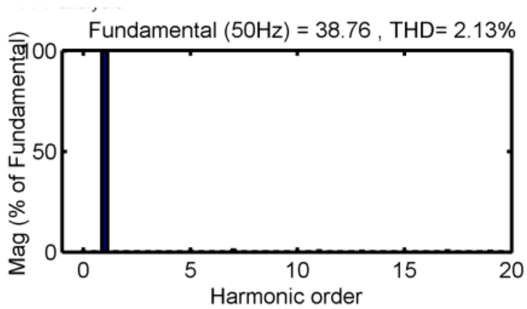

Fig. 9:. Source current with compensation

8. Conclusion

A control scheme for high performance three-phase DSTATCOM with improved power factor and displacement factor has been proposed. The remunerating execution of controller has been researched with various controller. The present control in view of hysteresis current controller has been executed. The simulated reaction demonstrates that the proposed control plans with T2FLC controller have a good performance in the harmonic compensation and improving the power factor, displacement factor and dynamic performance of the system.

References

[1] B. Singh, K. Al-Haddad and A. Chandra, "A review of active filters for power quality improvement," in IEEE Tran., on Ind. Electron., vol. 46, no. 5, pp. 960-971, Oct 1999.

[2] S. Buso, L. Malesani and P. Mattavelli, "Comparison of current control techniques for active filter applications," in IEEE Transactions on Industrial Electronics, vol. 45, no. 5, pp. 722-729, Oct 1998.

[3] Bhattacharya S., Banerjee and, Divan D. M., "Synchronous frameharmonic isolator using active series filter," in Proc. Eur. Power Electron.Conf., , pp. 3030–3035, 1991.

[4] S. Saad, L. Zellouma, "FLC for 3-level shunt active filter recompensing harmonics and reactive power," Electric Power Sys. Res., vol. 79, Is. 10, pp. 1337-1341, Oct. 2009.

[5] J. Li et al., "Three-level active neutral-point-clamped zero-current-transition converter for sustainable energy systems", IEEE Trans. Power Electron., vol. 26, no. 12, pp. 3680-3693, Dec. 2011.

[6] Xiao Peng, Venayagamoorthy GK, Corzine KA, "Seven-level shunt active filter for high power drive systems," IEEE Trans., Power Electron., vol. 24, no.1, pp. 6-13, 2009.

[7] Wenjin Dai, Yongtao Dai and Min Wu, "A new study for harmonic suppression and reactive power compensation," Industrial Technology, in proc., IEEE ICIT 2008, vol., no., pp.1,6, 21-24 April 2008

[8] B. Singh, V. Verma, and J. Solanki, "NN -based selective compensation current quality problems in distribution system," IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 53–60, Feb. 2007.

[9] Dhanavath Suresh, S.P. Singh, "design of single input FLC for shunt DSTATCOM," IETE journal of research, vol.61, no.5, 2016.

[10] Karnik, N. N., Mendel, J. M., and Qilian, L., "Type-2 fuzzy logic systems," IEEE Trans. Fuzzy Syst., Vol. 7, pp. 643–658,1999.

[11] Y. Jiao, S. Lu, F. C. Lee, "Switching performance optimization of a high-power high frequency 3-level active neutral point clamped phase leg building block", IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3255-3266, Jul. 2014.

[12] Yun-Liang Wang, Ming Bao, "A Variable Step-Size LMS Algorithm of Harmonic Current Detection Based on Fuzzy Inference," in proc. Of Computer and automation Engineering, vol. 2, pp.665-668, 2010.