International Journal of Engineering & Technology, 7 (3.29) (2018) 769-774

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Realization and Synthesis of 4 - bit Universal Shift Register using Logical Reversible Computation in Xilinx

Gopi Chand Naguboina[1*], K. Anusudha[2], T. Sravya [3]

[1] Department of Electronics and Communication Engineering, MVGR College of Engineering(A), Vizianagaram, India ,
[2] Department of Electronics Engineering, Pondicherry University Pondicherry, India,
[3]Department of Electrical and Electronics Engineering, Sri Padmavati Mahila Visvavidyalayam, Tirupati, India
**Corresponding Author E-mail: ngopichandmtech@gmail.com*

Abstract

Reversible Logic is the dominating field of research in low power VLSI. In recent times reversible logic has gained special attention in order to reduce power consumption mainly in concern to digital logic design. The main aim of this paper is to realize and synthesize universal shift register using reversible logic. Universal shift register is a sequential circuit that performs all the shift operations depending upon the selection lines. Different shifting operations performed using universal shift register are Shift left operation, shift right operation, parallel loading operation and no change operation. These operations are performed by the intervention of multiplexer circuit which helps to select the mode of operation to be performed. Hence a multiplexer is also designed using reversible logic to reduce power dissipation. Shift registers has their applications in data conversions like serial to parallel and parallel to serial conversions. A Boolean function f(i_1, i_2, i_3,……, i_n) having 'n' inputs and 'm' outputs is said to be logically reversible if the number of input lines are equal to the number of output lines(i.e. n = m) and the input line pattern maps uniquely the output line pattern. Few reversible logic gates in the existing literature are NOT gate, CNOT gate), Double Feynman (D2F) Gate, Peres Gate, TR gate, Seynman Gate etc. The logical reversible gates are designed such that they run both forward and backward directions and with the knowledge of output values, the input values can be also retrieved. The two limitations of logical reversibility is that Fan-out and Feed-back are not allowed. Certain output lines can be duplicated to desired number of lines using additional logical reversibly computed combinational circuits to overcome the Fan out limitation. Logical reversibility has applications in various areas like Nano- technology, optical computing, quantum computing, Computer Graphics, low power VLSI etc., Logical reversible computing has gained essence in recent times largely due to its property of low power consumption and low heat/power dissipation. In this paper, shift registers like shift right register, shift left register and universal shift registers which possess less power/heat dissipation and consumes less power is been proposed. The designed logical reversible computed circuits are analyzed in terms of quantum cost, garbage outputs and number of gates. The Circuits are been designed and simulated using Xilinx software.

Keywords: *Reversible logic, shift registers, universal shift registers, quantum cost, garbage outputs.*

1. Introduction

When logical computations with minimal energy dissipation are considered, logical reversibility plays a fundamental role. It was proved that reversible logical computation has a distinctive feature that it conserves information bits instead of erasing those bits. Power is an important factor to be considered along with time delay and area. The power consumption/heat dissipation will be very less in reversible logically computed circuits when compared with the irreversible logical circuits. According to Ralf landauer's (1961) Principle[1] erasing of each information bit causes KTln2 J of heat/power dissipation where K is Boltzman constant which is equal to 1.3805×10^-23 J/T and T is temperature. He proved that heat dissipation is not due to the process undergone in logical computation, it is due to wiping of bits in the process. This heat/power dissipation may be very small if a single Information bit is considered, but in very high complex VLSI circuits where large numbers of transistors are placed on a single chip, this type wiping of bits occurs at large amounts. It is predominant to understand that there exists a direct relationship between the number bits erased to the amount of heat/power dissipation occured. Later H.Bennet (1973) [2] proved that this type of heat dissipation can be reduced through logical reversible computation. Quantum logic gates are used to design reversible quantum circuits. Bennett argued that KTln2 joules of heat/power dissipation can be prevented if the logical computation is performed using reversible logical computation. Logical computation using reversible logical computation doesn't require erasing of information bits. This paper mainly concentrates on the realization of Universal shift register using logical reversible computation. Universal shift register is designed using a multiplexer (designed using logical reversible computation) which selects desired operation to be performed by the universal shift register.

2. Motivation

The practical limitation for high performance chips is heat dissipation. Moore's law states that the number of transistors integrated over the chip must be doubled every year as the chip size reduces to half. VLSI has already reached nanometer

technology and the researchers have been predicting that the road map of Moore's law will no longer be satisfied since the transistor size cannot be reduced further without falling into the leakage problems. Therefore the operating voltage levels cannot be scaled down than current levels. Therefore, Reversible logical computation gives an impressive solution that if the number of information bits are left without wiping, improvement of energy efficiency is possible. The conserved information bits are left un-computed. The un-computed left away bits are called garbage bits. The importance of Reversible computation cannot be ignored, even though the hardware complexity increases with it. With reversible computation, energy dissipation/consumption can be reduced or even can be eliminated if computation becomes information loss less.

3. Concept

Reversible logic Gates are used in logical reversible computing which contain the same number of input and output lines; also there should be one to one mapping between input and output vectors. In logical reversible computation [2], the reversible logic gates run in both forward and backward directions. If the designed circuit obeys both the above two conditions, then it satisfies the second law of thermodynamics which conserves the information bits without getting erased. Hence logical reversibility guarantees no heat dissipation and less heat/power consumption. Certain limitations are to be taken into account when designing circuits using logical reversible computation (i) Logical reversible computation does not allow Fan out and (ii) Logical reversible computation does not allow Feed – back also. In logical Reversible computation using outputs we can get the full knowledge of inputs. Certain output lines that are required to drive the inputs of consecutive device are duplicated into desired number of lines by using additional reversible logical computed combinational circuits to overcome the Fan-out limitation. Similarly Feed-back limitation can be overcome by making use of delay elements where feed-back is necessary. There are few cost metrics [5][4] associated with logical reversible computation. The performance of logical reversible computed circuits can be estimated by using the metrics such as Garbage outputs, Number of gates, constant inputs and Quantum cost. Garbage outputs are the unwanted extra outputs that help in making inputs and outputs equal in number in order to maintain logical reversibility. They are left ideal without any involvement in logical operation. Number of gates count will not be termed as a good metric since more number of reversible logic gates may be brought together to form a new reversible logic gate. Quantum Cost is nothing but the number of elementary or primitive reversible logic gates (or CNOT and NOT Gates) required to implement a new reversible logic gate. It is nothing but the number of reversible logic gates (1×1 or 2×2) required to construct the reversible logical computed circuit. The quantum cost has its identity in reversible logical computation. The area under the reversible logical computed circuit increases if the quantum cost is increased, which in turn increases the propagation delay. But quantum cost doesn't affect power/heat dissipation. Propagation delay is one of the important performance metrics.

4. Basic Reversible Logic Gates

The Schematic of Reversible Logic Gate which contains same number of inputs and outputs is shown in the below fig1. In the Existing literature there are few basic reversible logic gates mentioned below and a short note on each gate is given below. The reversible logic gates which are suitable for the desired logical design are considered. The reversible logic gates present in the existing literature are NOT Gate, CNOT[4], Double Feynman Gate [4], Toffoli Gate [8], Fredkin Gate [12], Peres Gate [5], TR Gate [5] etc., Among all the above listed reversible logic gates, NOT Gate is a 1×1 reversible logic gate which is basically an elementary or primitive gate. It just complements the given input and shifts it to the output. NOT gate's quantum cost is zero. CNOT gate is a 2×2 reversible primitive logic gate which is also a preliminary elementary gate. CNOT gate is also called as Feynman Gate. The quantum cost CNOT Gate is 1. These NOT and CNOT gates are the basic primitive gates which involve in realization of new reversible logic gates. The CNOT gate is used to duplicate a single line into two duplicate lines as reversible logic does not allow fan-out.

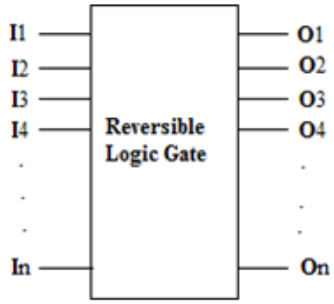


Fig.1: Schematic of simple reversible logic gate

The schematic and truth tables of both NOT Gate and CNOT gate are shown in the below figures.

Fig. 2: NOT Gate

Table 1: NOT Gate Truth Table

A	P
0	1
1	0

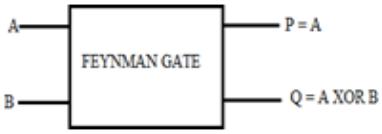


Fig. 3: CNOT Gate

Table 2: CNOT Gate Truth Table

A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

There are different types of 3×3reversible logic gates. The output vector O (P, Q, R) of each reversible logic gate is defined as the function of input vector I (A, B, C) as shown in the below figures.

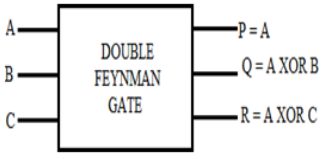


Fig.4: Double Feynman Gate

Table 3: F2G Gate Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

The Quantum Cost of F2G Gate is 2.

Table 4: Toffoli Gate Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

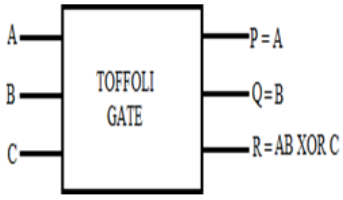


Fig.5: Toffoli Gate

Toffoli Gate's Quantum Cost is 4.

Table 5: Fredkin Gate Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

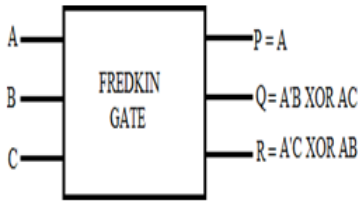


Fig.6: Fredkin Gate

The Quantum Cost of Fredkin Gate is 5.

Table 6: Peres Gate Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

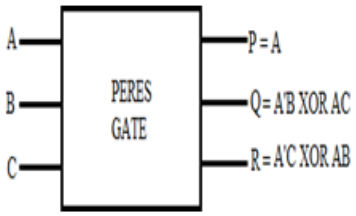


Fig.7: Peres Gate

The Quantum Cost of Peres Gate is 4.

Table 7: TR Gate Truth Table

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

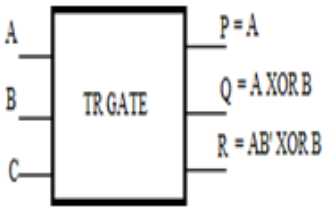


Fig.8: TR Gate

The Quantum Cost of TR Gate is 4.

V. Realization of Basic Gates, Multiplexer and D Flip – Flop Using Reversible Logic Gates

In concern with the circuit requirements, the basic gates like AND Gate and OR Gate can be realized using reversible logic gates as shown below. The 'R' output of fredkin gate gives the AND gate operation when it's 'C' input is driven with 0. Similarly the 'Q' output of fredkin gate gives the OR gate operation when it's 'C' input is driven with 1.

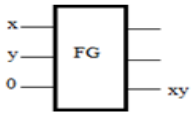
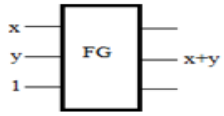


Fig.9 (a): AND Gate using fredkin



(b) OR Gate using fredkin

Similarly a multiplexer can also be realized using a Fredkin Gate. The reversible multiplexer designed using fredkin gate is as shown below.

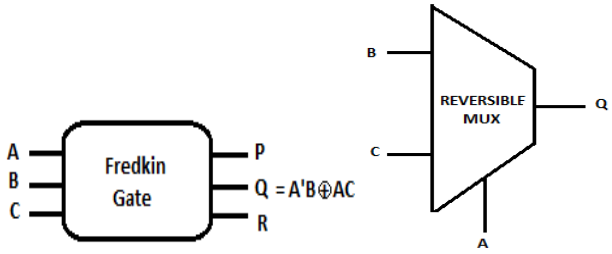


Fig.10: Fredkin Gate realized as 2×1 multiplexer

The 'Q' output of fredkin gate gives the min term expression of 2×1 multiplexer if 'A' input of fredkin gate is considered as selection line and 'B', 'C' inputs are considered as inputs lines. 'P', 'Q' lines are left ideal without usage. These are termed as garbage outputs. Here fredkin gate is considered to realize multiplexer because it gives better performance with acceptable Quantum Cost. In universal shift register an AND-OR gate combinational circuit is used to select desired shift operation. Here that AND-OR gate circuit can be replaced with a multiplexer made of reversible logic gates.

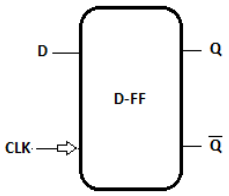


Fig.11: D Flip-flop

Table 8: Truth Table of D Flip-

CLK	D	Q	Q'
0	0	Q	Q'
0	1	Q	Q'
1	0	0	1
1	1	1	0

In general D Flip flop is used to design shift registers. The block diagram of D-FF and its truth table is drawn in the above figures. The characteristic equation of D-FF is

$$Q(t+1) = D \quad (1)$$

The excitation table of D-FF is as shown below. Excitation table gives the knowledge of inputs from possible combinations of outputs.

Table 9: Excitation Table of D Flip-Flop

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

A min term expression can be written for D as a function of Q (t) and Q (t+1) from the above table.

$$D = Q(t+1) \quad (2)$$

In order to realize a D flip-flop using suitable reversible logic gates, the above min term expression (2) is considered. Here a fredkin (F) gate and CNOT gate or Feynman gate is used to realize a reversible D Flip-flop. Feynman gate (FG) is used to overcome

feedback/Fan-out limitation of reversible logic. The proposed D Flip-flop using reversible logic is shown below.

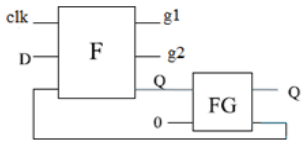


Fig.12: Proposed Reversible D Flip-flop

5. Proposed Revesible Shift Registers

In the existing literature flip-flops are designed using different types of reversible logic gates like RM Gate, seynman Gate etc. In this paper an attempt is made to realize D Flip-flop using basic reversible logic gates like fredkin and CNOT gate that have less quantum cost which are further used to design shift registers like shift right register, shift left register and universal shift register. The block diagrams of different 4-bit shift registers using reversible logic is depicted below.

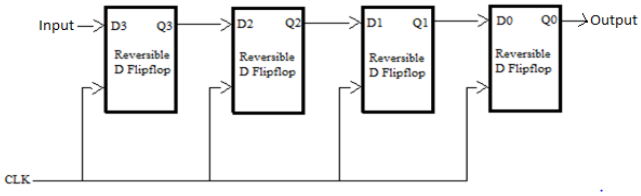


Fig.13: Proposed Shift Right Register using reversible D Flip-flop

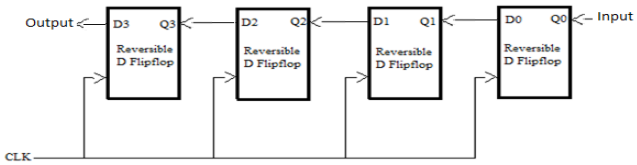


Fig.14: Proposed Shift Left Register using reversible D Flip-flop

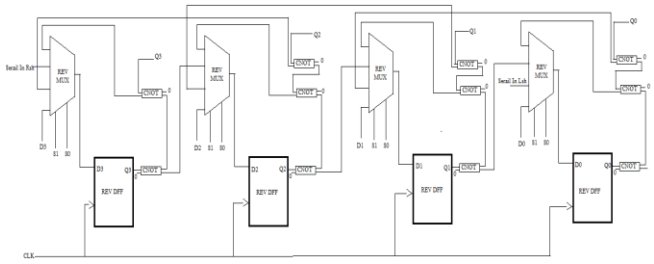


Fig.15: Proposed Universal Shift Register using reversible Logic

The shifting operations are performed by the intervention of a multiplexer circuit. Therefore a multiplexer using reversible logic with less quantum cost is designed which is used to select the mode of operation. The D flip flop proposed in the fig.12 is used to design the reversible logic computed shift register circuits. The circuit diagram of universal shift register using reversible logical computation is depicted in fig.15. The reversible logic gates selected in realizing the above shift registers are of minimum quantum cost with optimistic performance.

6. Simulation Results of Proposed Reversible Shift Registers

The simulation results of D-FF, shift left register, Shift right register and universal shift register designed using reversible logic are shown in the below figures 16, 17, 18, 19, 20 respectively. Figure 16 is the RTL schematic of reversible logical computed D – Flip-flop. From the below fig.17, it is very clear that for every clock pulse, the data given at the input end gets transferred to the output terminal. Hence the D flip flop operation does.

1) Simulation results of proposed D-FF using reversible logic:

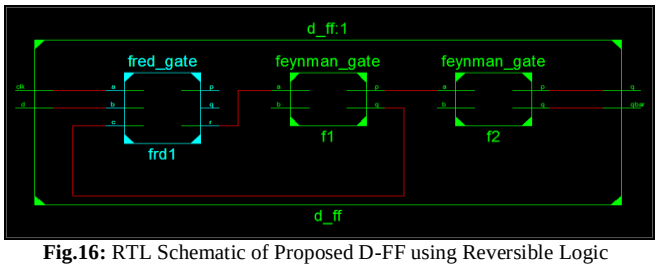


Fig.16: RTL Schematic of Proposed D-FF using Reversible Logic

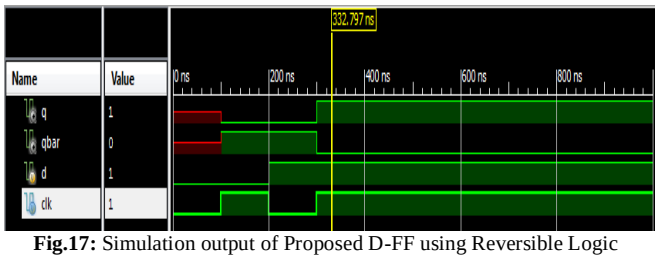


Fig.17: Simulation output of Proposed D-FF using Reversible Logic

2) Simulation outputs of proposed Shift Registers using reversible logic:

Fig.18: Simulation output of Proposed Shift Left Register using Reversible Logic

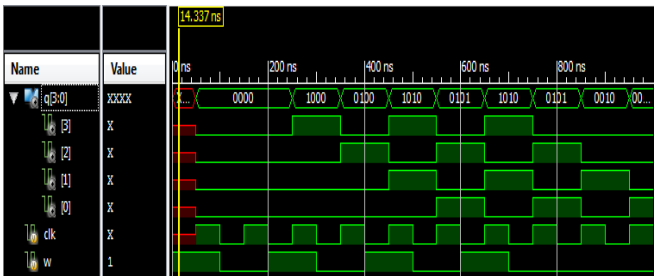


Fig.19: Simulation output of Proposed Shift right Register using Reversible Logic

From the above two simulation outputs in fig.18 and fig.19, it can be clearly noticed that for every input clock pulse the desired shifting operation is performed. From fig.18, it can be noticed that the bits are getting shifted from Q[3] to Q[0] accordingly for every clock pulse. The same type of shifting operation i.e. shift right operation is held from Q[0] to Q[3] in fig.19

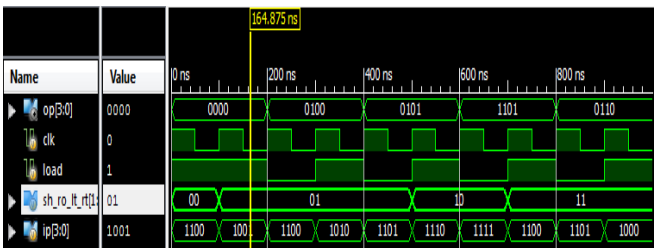


Fig.20: Simulation output of Proposed Universal Shift Register using Reversible Logic

From the above simulation output in fig.20, it can be noticed that shifting operations like shift left, shift right, parallel loading, no change operations are held according to the input selection lines. For 00 Selection inputs, No change operation is held. For 01 Selection inputs, shift right operation is held. For 10 Selection inputs, shift left operation is held and for 11 Selection inputs, parallel loading operation is held.

7. Analysis and Comparative Study

In the below table 10 different reversible logic gates used to build flip-flops are listed along with their Quantum Costs (QC).

Table 10: Different reversible logic gates with their QC

S NO	Reversible Logic Gate	QC
1.	Seynman Gate[16]	6
2.	Fredkin Gate[12]	5
3.	Peres Gate[5]	4
4.	Feynman Gate[4]	1
5.	RM Gate[14]	7
6.	RMCG Gate[15]	12
7.	RSJ Gate[14]	4
8.	SMBD Gate[16]	9

The below Table 11 gives the comparison of proposed D-FF using reversible logic with existing models in terms of Quantum cost (QC), Garbage Outputs(GO) and Constant Inputs(CI). The quantum cost of the proposed DFF is less when compared with the remaining existing models. The gates that were used to design DFF in each existing and proposed models are listed along with their respective quantum cost, garbage outputs and constant inputs. It is very clear that the proposed DFF's quantum cost is less which in turn possesses less propagation delay.

Table 11: Comparison of proposed D-FF with existing models

	Gates Used – No's	**QC**	**GO**	**CI**
Existing Model[17]	FRG -4 PG - 4	9	3	2
Existing Model[16]	SMBDG - 1, FG -1	11	4	2
Proposed Model	FRDG -1, FG - 1	6	2	1

The below table 12 give the comparison of proposed shift registers designed using logical reversible computation with the existing shift registers designed with reversible logic. It is very clear that the quantum cost of every proposed reversible shift register is reduced when compared with the existing circuits. Hence the quantum cost is reduced and garbage outputs were also reduced where ever it is possible.

Table 12: Comparative study of Reversible shift registers

Reversible Device	**Gates Used - No's**		**Parameter**	**Existing**	**Proposed**
	Existing	Proposed			
Shift Left Register	FRG - 4, PG - 4	FRG - 4, FG - 4	QC	36	24
			GO	12	8
Shift Right Register	FRG - 4, PG - 4	FRG - 4, FG - 4	QC	36	24
			GO	12	8
Universal Shift Register	-	FRG- 16, FG - 15	QC	–	95
			GO	–	32

8. Summary

From the performance analysis it is clear that all the shift registers are designed with minimum quantum cost and minimum garbage outputs. The designed circuits are simulated and are analyzed in terms of propagation delay. If the quantum cost and garbage outputs are more, then it is clear that the area of the circuit increases which implies increases propagation delay also. It is observed that the propagation delay of reversible circuits is slightly higher than the irreversible circuit which is negligible. This can be termed as disadvantage of these designs. It will be really an achievement if the reversible circuits designed possess less propagation delay when compared with the irreversible circuits. Despite of this demerit the importance of reversible circuits cannot be neglected because of the efficiency in terms of heat dissipation/power consumption. Eighty percentage of heat efficiency can be obtained by using reversible logic.

9. Future Scope

The future scope for this paper is, the circuits that are designed can be implemented more precisely with less quantum cost and less garbage outputs, so that the propagation delay and area can also be reduced.

10. Conclusion

The proposed shift registers designed using reversible logical computation is designed with minimum quantum cost. If the quantum cost and garbage outputs are more, then it is clear that the area of the circuit increases which implies increase in propagation delay also. In general the propagation delay is slightly more in reversible logic circuits when compared with the irreversible logic circuits. But it will be really an achievement if the propagation delay was reduced in reversible logical computed circuit than the irreversible circuits. The propagation delay of reversible shift register and irreversible shift register is 2.371nsec and 2.23nsec respectively. In the existing models flip flops are designed using derived reversible logic gates in which quantum cost is more whereas the flip flops proposed are designed using basic reversible logic gates with minimum quantum cost. These logical reversible computed flip flops are used to design shift registers in which quantum cost is reduced when compared with existing models. In this paper a universal shift register is proposed using logical reversible computation which is not implemented earlier in the existing literature.

References

[1] R. Landauer, ―Irreversibility and Heat Generation in the Computational Process‖, IBM Journal of Research and Development, 5, pp. 183- 191, 1961.

[2] C.H. Bennett, ―Logical Reversibility of Computation‖, IBM J.Research and Development, pp. 525-532, November 1973.

[3] C H Bennett, "Notes on the History of Reversible Computation", IBM Journal of Research and Development,vol. 32, pp. 16-23, 1998.

[4] R. Feynman,‖quantum mechanical computers:, Optic News, vol. 11,pp 11-20, 1985.

[5] A. Peres, ―Reversible logic and quantum computers‖, phys.rev.A,Gen.Phys., vol. 32, no. 6, pp. 32663276, Dec. 1985.

[6] H.G Rangaraju, U. Venugopal, K.N. Muralidhara, K. B. Raja,‖Low power reversible parallel binary adder/subtractor‖ arXiv.org/1009.6218,2010.

[7] J.M. Rabaey and M. Pedram, ―Low Power Design Methodologies,‖ Kluwer Academic Publisher, 1997.

[8] T. Toffoli., ―Reversible Computing‖, Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.

[9] Y. Syamala, and A. V. N. Tilak, ―Reversible Arithmetic Logic Unit‖, Electronics Computer Technology (ICECT), 2011 3rd International, vol. 5, pp.207-211,07 july 2011.
[10] Thapliyal H, Ranganathan N.,‖ Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs‖ Centre for VLSI and Embedded .
[11] V.Rajmohan, V.Ranganathan,‖Design of counter using reversible logic‖ 978-1-4244-8679-3/11/$26.00 ©2011 IEEE.
[12] Vivek V. Shende, Aditya K. Prasad, Igor L. Markov, and John P. Hayes,‖ Synthesis of Reversible Logic Circuits‖, IEEE Transaction on computer-aided design of integrated circuits and systems, vol. 22, No. 6, June 2003.
[13] Payal Garg, Sandeep Saini,"A novel design of compact reversible SG gate and its applications‖,2014 14th International Symposium on Communications and Information Technologies(ISCIT), Sept 2014, pages 400-403, doi: 10.1109/ISCIT.2014.7011941
[14] V. Rajmohan, V. Ranganathan, "Design of counters using reversible logic", 3rd International Conference on Electronics Computer Technology, 978-1-4244-8679- 3/11/$26.00 ©2011 IEEE.
[15] Shefali Mamataj, Biswajit Das, Saravanam Chandran, "An Approach for Designing of Sequence Generator by Counter and Multiplexer of Reversible Gates", International Conference on Contemporary Computing and Informatics – (IC3I – 2014), 978-1-4799-6629-5/14/$31.00_c 2014 IEEE.
[16] Shefali Mamataj, Biswajit Das, "Efficient Designing Approach of Different Synchronous Cyclic Code Counters by Sequential Circuits Elements of a Novel Reversible Gate", Sixth International Conference on Computational Intelligence and Communication Networks" - (ICCICN – 2014) ,978-1-4799-6929-6/14 $31.00 © 2014 IEEE.
[17] D.Santhiya, D.N.Keerthi Kumar, "Testable Circuit for Universal Shift Register Using Reversible Gates",International Journal for Innovative Research and studies,ISSN 2319-9725,Volume3, Issue5, may 2014.
[18] Jadav ChandraDas, Debashis De and Tapatosh Sadu.‖ A novel low power nano scale reversible decoder using quantum dot cellular automata for nano communication‖, Third International Conferrence on devices, circuits and systems, 2016.
[19] Ritjit Maumdar, sandeep saini ― A novel design of reversible 2: 4 decoder‖,978-1-4799-6761-2/$31.00©2015 IEEE
[20] Rupali Singh, Manoj Kumar Pandey, "Design and Optimization of Sequential Counters Using A Novel Reversible Gate", International Conference on Computing Communication and Automation" – (ICCCA - 2016), 978-1-5090-1666-2/16/$31.00 ©2016 IEEE.
[21] Gopi Chand Naguboina, K. Anusudha, "Design and synthesis of combinational circuits using reversible decoder in Xilinx" – International Conference on Computer, Communication and Signal Processing (ICCCSP -17) , 978-1-5090-3716-2/17/$31.00 ©2017 IEEE.
[22] Gopi Chand Naguboina, K. Anusudha, "Design and Implementation of Programmable Read Only Memory using reversible decoder on FPGA" – International Conference on Signal Processing, Communications and Networking, (ICSCN – 17), 978-1-5090-4740-6/17/$31.00 ©2017 IEEE.
[23] Gopi Chand Naguboina, K. Anusudha, "Design and Implementation of PAL and PLA using Reversible Logic on FPGA Spartan 3E" – International Conference on Signal Processing, Communications and Networking (ICSCN - 2017), 978-1-5090-4740-6/17/$31.00 ©2017 IEEE.
[24] Gopi Chand Naguboina, K. Anusudha, "Design and Implementation of BCD to Seven Segment Display Decoder using reversible decoder on FPGA", International Journal of Computing and Applications, Volume 13, Number 2, (March - April 2018), pp 265-275© Serials Publications, New Delhi (India), ISSN: 0973-5704.