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Research paper

"Exploration of power delay product [PDP] on feedback based dual edge triggered flip flop utilizing dual sleep and dual slack approach"

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Abstract

In Modern Digital electronics, the low power circuits become the essential part. As the flip-flops are basic storage components utilized as a part of significant number of digital circuits, so they must be planned with upgraded power consumption. Power dissipation is the important factor in Dual Edge Triggered flip flop. Low glitch and low power DET flip-flops are based on a feedback element utilizing dual sleep and dual slack approach are proposed to keep up a steady throughput while working at half clock frequency. Feedback elements are utilized to reduce the switching activities because of input signal transitions. In the proposed design the internal nodes will not respond to input signal variations. As the innovation is scaling from micron technology to profound submicron technology the leakage power is one of the parameter which impacts the circuit execution, by utilizing these dual sleep and dual slack techniques are proposed and compared to existing DET flip-flop designs utilizing 45nm CMOS technology. The simulation result demonstrates that Conditional Toggle flip-flop using dual sleep and dual slack techniques shows better Power Delay Product (PDP).

Keywords: *C-Element; Dual-Edge-Triggered; Flip-Flops; Dual Sleep; Dual Slack; Low Power.*

1. Introduction

Generally, flip-flops and latches are used as regularly as possible utilized segments to store the information and have incredible potential in digital electronics. In synchronous frameworks, most extreme speed is chosen by beginning and ending of signal delay paths. To lock the information, it requires a positive or negative clock pulse. Dual Edge Triggered methods [2] are picking up noticeable quality to decrease unnecessary power dissipation. It reacts to raise clock edge as well as fall clock edges. The information rate of the DET flip-flops is two times higher when compared SET flip-flop [3]. This change enables these flip-flops to be timed at 50% of the frequency, thus reducing the power consumption by half. The DET flip-flop is nothing but a Latch-MUX flip-flop which are level triggered by opposite clocks, output of these latches are multiplexed to the final output stage through a multiplexer as shown in the Figure.1. Within the sight of the glitches at the input, the power utilization of the flip-flops will be significantly affected by these glitches. Glitches will affect the power consumed by flip-flops. The other form of DET flip flop design is Conditional toggle flip-flop which reduces the unfavorable impact of information glitches at the output.

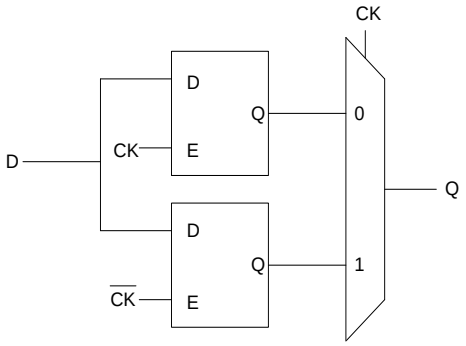

Fig. 1: Latch MUX Flip-Flop [1].

This paper exhibit new flip-flops designs which depend on feedback elements based DET flip-flops using dual sleep and dual slack techniques. This paper has four segments. Section I is Introduction that presents the basic knowledge of DET flip-flops, Section II presents the DET flip-flop designs that uses the C-element. CT_C flip-flop using dual sleep and dual slack techniques are included in this section, Section III presents existing flip-flops and the comparison methods of existing design with proposed designs and lastly Section IV finishes up this paper.

2. Circuit description

Muller presented a three terminal gadget called C-component [6] which has two data sources A and B and one output C. Logic behavior of the circuit is the output switches to value of the inputs when both inputs are same; the previous output value is stored, when inputs are not same. The C component produces the output which is equal to the input when the two input signals are similar. When the two input signals are not equal, the previous data values will be stored.

These components are utilized as a part of outlining of flip-flop and latches. In this paper, we utilize weak-feedback and dynamic C-components, which are the essential building pieces of new DET flip-flops as appeared in Figure.2

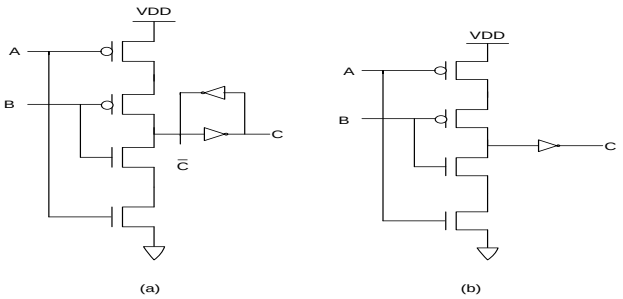

Fig. 2: A) Structure of the C Feedback Element [6] B) Dynamic Element Structure [6].

The power consumption is high in this Latch-MUX design, so the design is modified to conditional toggle c-element based flip flop which results in power consumption. The transistor level structure of the above design is shown in Figure 3.This design is having a total of only 20 transistors. The inputs to CT_C flip-flop are designated as D and CK and the output is referred as Q. The output of the CT_C flip-flop is clearly shown in the Figure 4. As the circuits are designed in sub-micron technology, the leakage power consumption is high so in order to reduce the leakage power extra circuitry is added to this CT_C flip-flop.

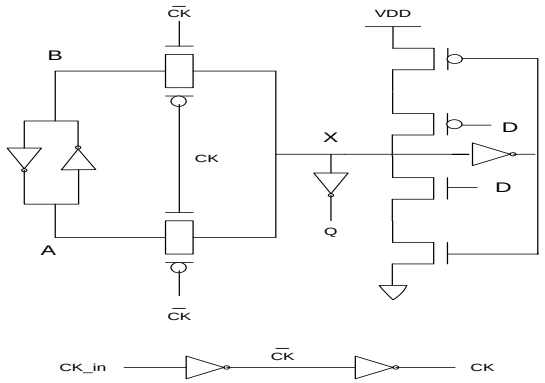

Fig. 3: Transistor Level Implementation of Conditional-Toggle CT_C DET Flip-Flop.

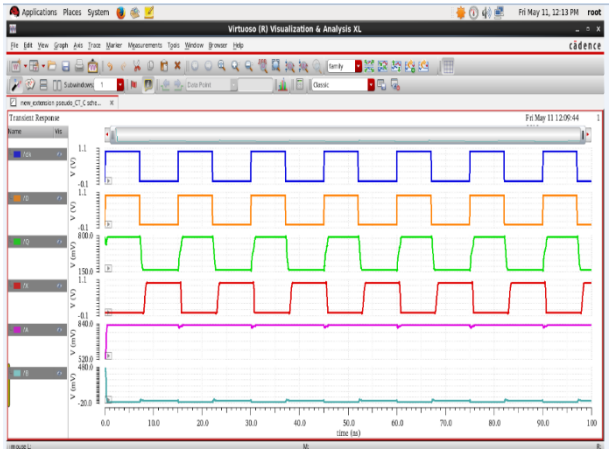

Fig. 4: Operational Waveforms of CT_C Flip-Flop.

3. CT_C flip-flop using dual sleep technique

The transistor level schematic of dual sleep technique is as shown in the Figure.5, The Conditional Toggle (CT_C) flip-flop is improved by adding extra circuitry with one NMOS and one PMOS transistor which are connected in parallel at both VDD and GND for creating virtual VDD and virtual GND for by passing the leakage current. The sleep transistors are driven by opposite clocks CK1 and CK1B. When D becomes equal to CK and CKB the internal nodes A and B switches to CKB and CK respectively. At least one the node A or B should be DB in between the clock transitions. The output Q switches to D after every clock transition when both A and B are equal to QB. Although the number of transistors is increased (4 transistors are addition added) when compared to CT_C flip-flop the power dissipation has reduced considerably.

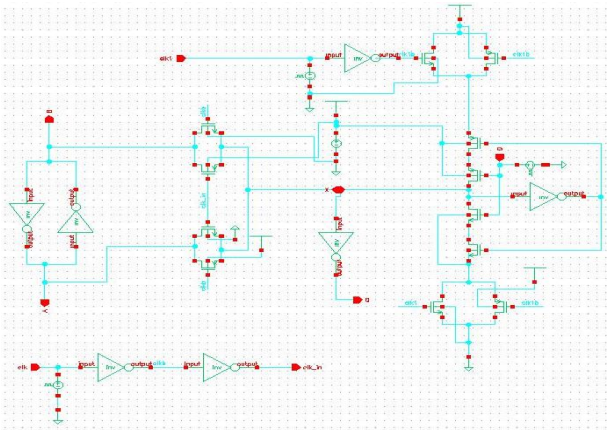

Fig. 5: Structure of the CT_C Flip-Flop Using Dual Sleep Technique.

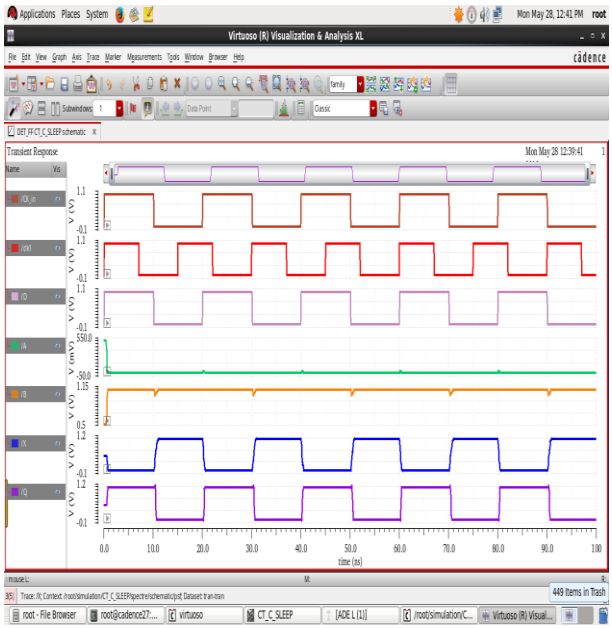

Fig. 6: Conditional Toggle Flip-Flop Structure Using Dual Sleep Technique.

4. CT_C flip-flop using dual slack technique

The transistor level schematic of dual slack technique is as shown in the Figure.7. Common circuitry is attached to logic circuitry with two slack transistors connected in series with one sleep transistor parallel at the VDD and GND. The circuitry at VDD comprises of one PMOS sleep transistor in parallel with two NMOS slack transistors connected in series. The circuitry at GND comprises of one NMOS sleep transistor in parallel with two PMOS slack transistors connected in series. The conditional toggle flip-flop operation using dual slack technique is similar as like CT_C flip-flop using dual sleep technique.

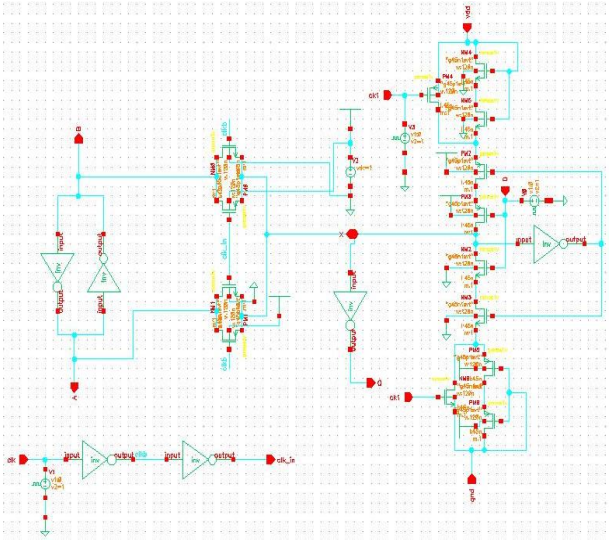

Fig. 7: The Structure of the CT_C Flip-Flop Using Dual Slack Technique.

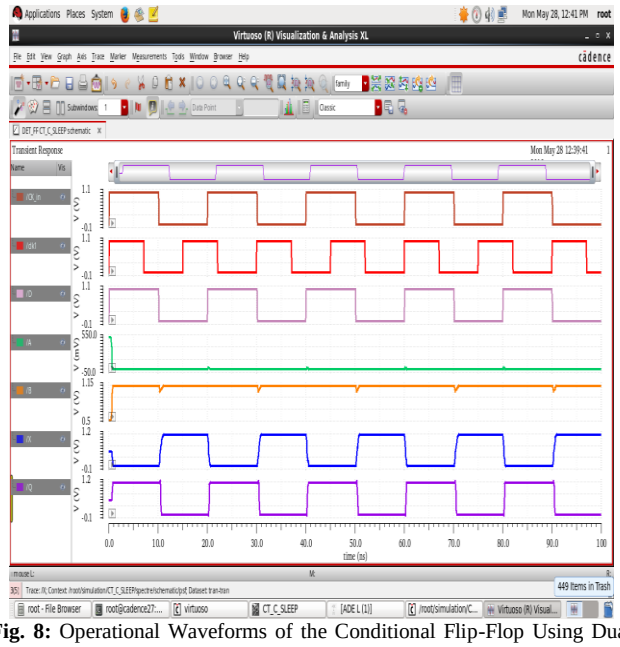

Fig. 8: Operational Waveforms of the Conditional Flip-Flop Using Dual Slack Technique.

The two sleep transistors are driven by the opposite clocks CK1 and CK1B respectively. The clock signal CK1 is only responsible for operating the sleep transistors and this will not alter the operation of the conditional toggle flip-flop. VDD is kept at high voltage and the GND is kept at low voltage for the two slack transistors. The drain induced barrier lowering which occurs in the deep sub-micron technology reduces by using this dual slack techniques and results in low leakage power and average power dissipation is reduced for CT_C flip-flop using dual slack technique when to the other flip-flops having higher performance.

5. Simulation results

The DET flip-flops which were presented were simulated in 45nm technology. The tool used for simulation, average power dissipation and delay calculation is cadence virtuoso software. DET flip-flop is designed using latch MUX. The latch MUX C-element [6] is an improved design of latch-MUX design (LM), where the C-element provides a substitute for MUX. The operation of this improved design does not change and will retain same as LM flip-flop. The LG-C, IP-C, CT-C, CTF-C flip-flops are C-element based designs which were presented in [1] are having lesser power dissipation and better power delay product. CT_C flip-flop is taken for further improvement and added dual sleep and dual lack techniques presented for reducing the power dissipation and achieved the superior results than the existing flip-flops.

Table 1: Comparison of Delay and Power of Different DET Flip- Flops in 45nm CMOS Technology

Name of the flip-flop	Power(us)	Delay(pHs)	PDP(fJ)
Latch-MUX Flip-flop [6]	3.187	489.0	1.558
LM_C Flip-flop [7]	2.821	594.8	1.677
LG_C DET Flip-flop	2.849	633.7	1.805
IP_C DET Flip-flop	2.515	505.4	1.271
CT_C DET Flip-flop	1.295	419.2	0.542
CTF_C DET Flip-flop	1.272	362.3	0.460
CT_C DET Flip-flop using dual sleep technique	0.944	420.2	0.396
CT_C DET Flip-flop using dual slack technique	0.745	440.4	0.328

6. Conclusion

Reducing the Sub threshold leakage power is one of the difficult tasks in CMOS scaling technology. The leakage power is reduced using dual sleep and dual slack techniques. As the Low power

VLSI circuits are having a great demand in digital electronics, The DET flip-flops reported here are used in a number of applications and can be used further for designing shift registers , counters and memories. Cadence is one of the best platforms for working on analog and digital circuits. The CT-C flip-flop using both dual sleep technique and dual slack technique are having high performance when compared to existing flip-flop. The circuits further can be designed and simulated using Finfet technology which would be more advantageous.

References

[1] Stephan Lapshev and S.M. Rezaul Hasan, "New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, June 2016.

[2] S.V. Devarapalli, P.Zarkesh-Ha, and S.C. Suddarth, "A robust and low power dual data rate (DDR) flip-flop using C-elements,"in Proc. 11thIntSymp. Quality Electron. Des. (ISQED), Mar. 22-24 2010, pp, 147-150.

[3] D.E Muller, "Theory of asynchronous circuits," Internal Rep. o 66, Digit. Comp L ab.,unit. Illinois at Urbana- Champaign, 1955.

[4] M. Shams, J.C. Ebergen, and MI Elmasry, "Modeling and comparing CMOS implementations of the C-element,"IEEE Trans. Very Large Scale integer. (VLSI)Syst., vol.6, no.4, pp.563-567, Dec.1998.

[5] R.Hossain, l... D Wronski, and A.Albicki, "Low power designs using double edge triggered flip-flops," IEEE Trans. Very Large Scale Intefr. (VLSI) Syst., vol.2, no.2, pp.261-265, Jun.1994.b.

[6] M. Pedram, Qing Wu, Xunwei Wu. "A new design of double edge triggered flip-flops", Proceedings of 1998 Asia and South Pacific Design Automation Conference, 1998. https://doi.org/10.1109/ASPDAC.1998.669513.

[7] Khan, Imran Ahmed, Danish Shaikh, and Mirza Tariq Beg. "2 GHz low power double edge triggered flipflop in 65nm CMOS technology", 2012 IEEE International Conference on Signal Processing Computing and Control, 2012 https://doi.org/10.1109/ISPCC.2012.6224375.