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Research paper

Design and Implementation of Low Power, Area Efficient Full Adder for High Performance Digital Circuit Applications

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Abstract:

Design and implementation of low power, low delay and area efficient full adder using new architecture of XOR-XNOR gates will be efficient than existing full adders. Design of hybrid 1-bit full adder circuits combined in a single circuit employing both complementary metal-oxide-semiconductor (CMOS) logic and transmission gate logic. The proposed architecture will consume less power consumption, transistor area and propagation delay and it is compared with existing design such as Complementary Pass Transistor Logic [CPL], Transmission Gate Full Adder [TGA], Transmission Function Adder [TFA], SERF and 14T full adder. Use of proposed adder, 8-bit array multiplier is designed and its performance is compared with CMOS architecture. The simulation of all designed structure is performed in Cadence Virtuoso Tools in 90-nm technology

Keywords: *Low power, Full Adder,XOR- XNOR GATE, Multiplier.*

1. Introduction

With the rapid growth in the VLSI (Very Large Scale Integration) semiconductor Technology, There is a need of high speed devices with less power consumption and capable of computing multiple operations at a time. So ultimately it can leads to an increase the number of transistor in an integrated circuit. Power and speed are the two most important design parameter objectives in integrated circuit. While designing a circuit, Designer should be aware of design constraints like power, delay and area. There is always a trade-off between power and delay. Getting the optimized value of both power and delay. Of the circuit is the challenging task for designer.

The basic operation of adder is the addition of binary numbers and it is the basic unit for many complex arithmetic operations like multiplication, division and exponentiation and it is used as basic block in multipliers, comparator and parity checker. The full adder is realised by using XOR, AND& OR gates. XOR/ XNOR gate is heart of the full adder circuit. Designing of XOR gate with minimal number of transistorinfluences the performance of the full adder circuit.

The Full adders are the building blocks of the ALU and MAC units of a processor. Marimuthu et.al., (2013) has proposed new multiplexer based 8-4,9-4 compressors for speeding up summation of partial products in a multiplier with reduced power consumption. The multiplexers exhibit reduced power consumption due to V_{dd} supply is not accessed like regular CMOS logic gates, so multiplexers are used to realize the XOR gate functions which can bring about a considerable reduction in power consumption of XOR based logics. Shin-Kai Chen et.al., (2013) has proposed an improved version of pipelined booth multiplier in which the partial product rows of a booth multiplier are split in to vertical columns and are reduced by means by Wallace tree reduction applying the concept of pipelining . Here the number of adder logics used in the multiplier is reduced and this leads to a more compact booth multiplier. Ron S. Waters et.al., (2010) proposed a method for reducing the routing complexity in a Wallace tree multiplier which may reduce the power consumption in Wallace tree realization due to the irregular routing. This concept involves reducing the number of Half adders used in a Wallace tree there by reducing the complexity involved in the routing between the intermediate adders.

Ramkumar et.al., (2012) proposed an area reduction methodology in SQRT CSLA by means of using a BEC (binary to excess 3 convertor). The logic is based on the fact the Output of the RCA with carry-0 can be converted to a RCA output with carry-1 by means of a BEC. The logic results in savings of area since BEC need lesser gates compared to RCA. YI WEI et.al., (2011) has proposed a novel 3T low power XOR gate by which a 8T adder can be synthesized and the Adder exhibits reduced power consumption since it doesn't access the power supply (Selvakumar et al., 2016) . The output from the adder suffers from threshold voltage degradation and this makes undesirable for usage in cascaded tree based multiplier structures.

Kathirvelu, M. and Manigandan, T., (2012) proposed a logical modification for 12T MBA that reduces the switching activity there by power consumption in a 12T MBA. The lower order multipliers can be efficiently synthesized by using the optimized improved 12T MBA. But that design needs keeper transistor along the cascaded stages. Ramkumar et.al., (2011) proposed a high speed Dadda multiplier using a hybrid for the final CPA addition in the Dadda multiplier. The CSLA based on BEC with minimized area overhead is used in the final stage of the Dadda multiplier.

Yiangtao jiang et.al., (2006) proposed a low power 12T MBA for low power addition. The adder is based on the use of the 6 two transistor multiplexer it exhibits reduced power consumption but suffers from threshold voltage degradation.(Hussin2008) proposed a modified booth multiplier with 4:2 compressors. The partial products are reduced by means of high speed compressors
leading to faster multiplication. (Shalem et.al, 1999) proposed a low power energy recovery full adder cell which was realized using 10 transistor which proved a better performance in terms of power and delay when compared to that of other 14T adders. The output waveforms of SERF suffer from threshold degradation hence may yield improper outputs when connected in a Carry Save Array based multiplier.

2. Hybrid Pass Logic with Static CMOS Output Drive Full Adder (HPSC)

The hybrid pass logic with static CMOS output drive full adder(HPSC) is shown in figure 1 is taken as reference adder. The sum output of the full adder is implemented by XNOR modules. The inverter comprised of transistors Mp1 and Mn1 generate B', which is effectively used to design the controlled inverter using the transistor pair Mp2 and Mn2. Output of this controlled inverter is basically the XNOR of A and B. But it has some voltage degradation problem, which has been removed using two pass transistors Mp3 and Mn3. pMOS transistors (Mp4, Mp5, and Mp6) and nMOS transistors (Mn4, Mn5, and Mn6) realize the second stage XNOR module to implement the complete SUM function.

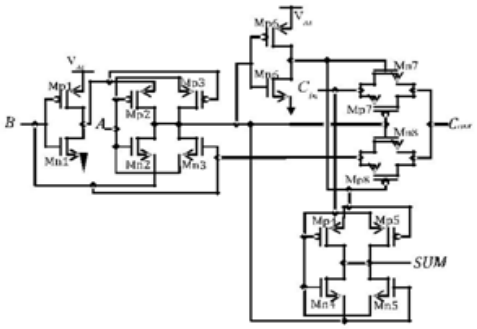

Figure 1: Hybrid pass logic with static CMOS output drive full adder (HPSC)

3. Proposed Full Adder

The design of the proposed adder circuit is represented by three blocks as shown in figure2. module 1 and module 2 are the XNOR modules that generate the sum signal (SUM) and module 3 generates the output carry signal (CARRY). The XOR/ XNOR reported in reference paper uses six transistors whereas the proposed adder uses four transistors. At the output stage pass transistor logic is used to reduce the power and delay. The proposed structure gives the same output with improved performance (MuhammedShafi et al.,2018) . The schematic of proposed adder is shown in figure 3.

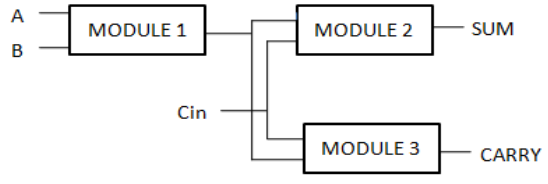

Figure 2:.Proposed full adder

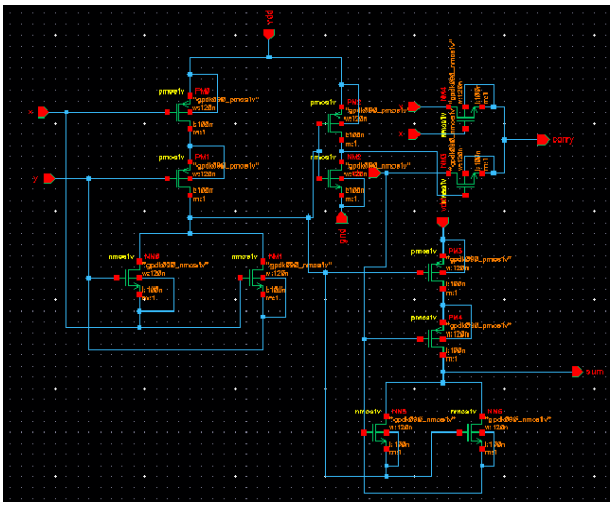

Figure 3: Schematic of Proposed full adder

3.1 Performance Comparision of Various Full Adders

The performance of various full adder is given in Table 1.

Design	Power (uW)	Delay(pS)	PDP in fj	No.of transistors
C-CMOS	0.069	266	0.018	28
10T	16.30	3.07	0.051	10
TGA	29.96	3.0	0.089	20
14T	36.37	291	10.583	14
SERF	7.97	200	1.594	10
HPSC	37.16	49	1.82	16
Proposed full adder	28.42	12.73	0.36	12

HPSC consumes more power than other adders. C-CMOS dissipates much low power compared to all adders. The power consumption of the proposed adder is less compared with the existing HPSC adder. Figure 4shows the power consumption of different types of adder.The 14T adder delay is more compared to all other adders. 10T and TGA delay is almost same and negligible. The delay of the proposed adder is less compared with the reference HPSC adder and is shown in figure 5. The power delay product (PDP) is to be low for high performance circuits. 14T produces higher PDP than all other architectures. C-CMOS require less PDP compared to all other adders with increase in transistor count. The PDP of proposed adder is low with compared to HPSC and is shown in figure 6.

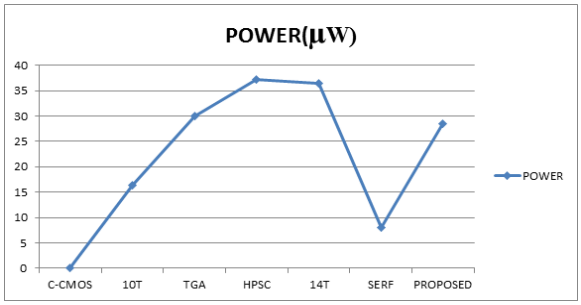

Figure 4 : Power Consumption of various adders

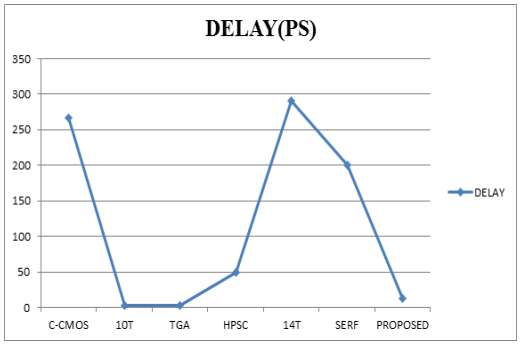

Figure 5: Delay of various adders

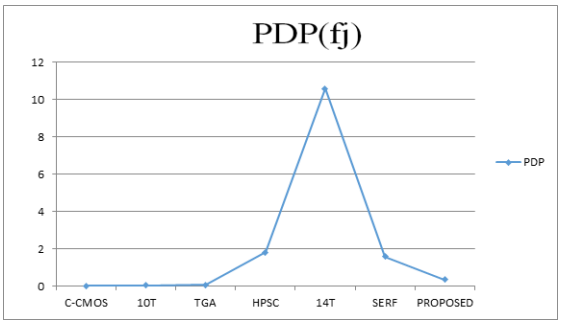

Figure 6: PDP of Different adders

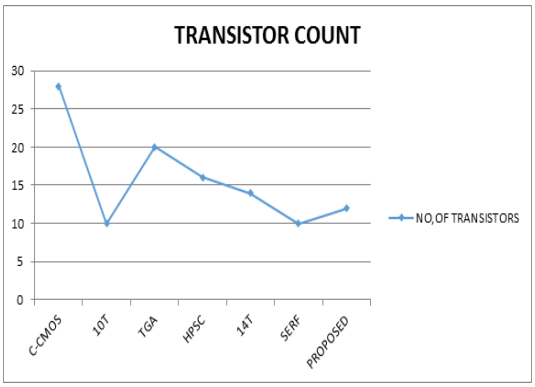

Figure 7: Architecture vs. transistors

The proposed adder will have 68% improved performance than reference adder. The proposed adder is used to implement 8 bit array multiplier.

4. Array Multiplier

Array multiplier is a digital combinational circuit that is used for the multiplication of two binary numbers by employing an array of full adders. This array is used for the nearly simultaneous addition of the various product terms involved. To form the various product terms, an array of AND gates is used before the adder array. The architecture is shown in figure 8 and its performance is given in table 2. The performance characteristics is shown in figure 9 &10.

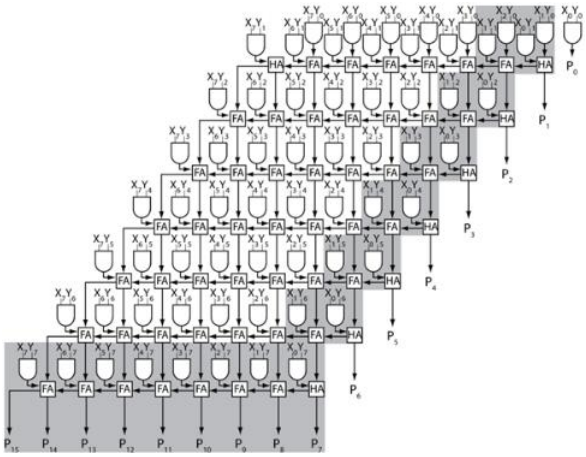

Figure 8: Architecture of 8*8 Array multiplier

4.1 Simulation results for 8*8 Array multiplier

S:NO	ARCHITECTURE	POWER (μw)	DELAY (ns)	PDP (fJ)	NO. OF TRANSISTORS
1.	8*8array Multiplier Using Hpsc Adder	743.2	52.3	38869.3	1280
2.	8*8 Array Multiplier Using Proposed Adder	486.4	43.06	20915	1056

The 8*8 array multiplier using proposed full adder offered 46.19% improvement with respect to the 8*8 multiplier using HPSC adder in terms of PDP.

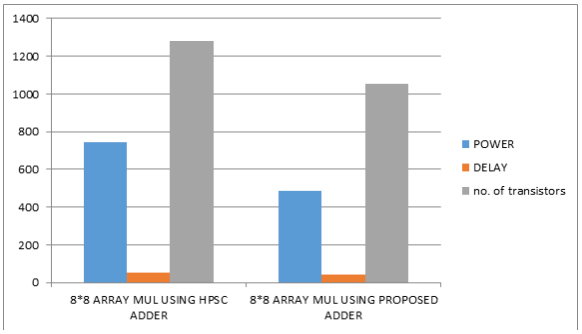

Figure 9: Comparison of power, delay and No. of transistor of 8 bit array multiplier

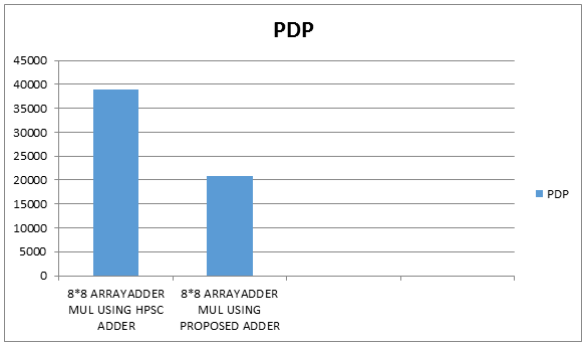

Figure 10: Comparison of PDP of 8*8 array multiplier

5. Conclusion

The different types of full adders have been simulated and its performance in terms of power,PDP, delay and No.of transistors is depicted. The proposed full adder is 68% better performance than HPSC adder. An 8 bit array is designed with proposed and HPSC adder and is simulated in 90 nm technology in cadence tool. The 8*8 array multiplier using proposed full adder offered 46.19% improvement with respect to the 8*8 multiplier using HPSC adder in terms of PDP.

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