Realization and Fabrication of 3rd Order High Pass Filter with CMOS

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Abstract

This research work encapsulates the early stages and recent stages of the third order high pass filter design process. The main objective of this work is to design and analyse the parameters of *third* order high pass filter using MOSFET technology. It has been designed by cascading a first order with a second order high pass filter. The filter has cut-off frequency of 1 GHz. The core building blocks of the third order high pass filter are the op-amps which are responsible for providing gain in the filter circuit. Therefore one of the typical LM741 op-amps in the filter circuit has been replaced with two-stage CMOS op-amp for enhanced CMRR, unity gain bandwidth, and reduced power consumption. This will allow the filter to operate for RF transceiver systems. The designed third order high pass filter has implemented to hardware at double sided design and displayed transient responses that are compared to the simulated results and achieved better filtering effect. The bandwidth of the designed filter is higher than the conventional 3rd order high-pass filter which is also simulated in this work.

Keywords – Third Order, filter, High-pass filter, MOSFET, CMOS, Differential amplifier, Fabrication.

1. Introduction

Filters which have active devices and are of high order are commonly applied in RF transceivers, satellite systems, and radar communication systems [1, 2]. These filters provide better dynamic range, high SNR, high stop-band attenuation, lower sensitivity and they are easily adjustable [3-5]. High-order filters can be designed using different methodologies including cascade, multiple-loop feedback, or the ladder simulation method [6, 7]. The transfer function in cascade method is formulated by cascading the first and second order filter sequence [8]. The advantage of this method is its simple design procedure [9-11].

Conventional analogue filters utilize active elements which consist of certain transistors and op-amps that increase the power consumption [12, 13]. The active and passive elements used in these analogue filters increase circuit complexity, insertion and operation losses [14]. Conventional filters require expensive external capacitor structures. The operating frequency in conventional passive RC filters is lower than transistor active based filters [15, 16].

Filters are generally classified by the function as four basic functions which is low-pass, high-pass, band-pass, and band-stop [17-19]. An ideal low pass filter is classified by its abilities to pass frequencies from zero to its cut-off frequency f_c and attenuate all frequencies higher than the cut-off frequencies. An ideal high pass filter passes all frequencies above the cut-off frequency and attenuates all frequencies below the cut-off frequency. A band stop filter stops all frequencies with a frequency range of f_1 and f_2 and passes all other frequencies outside of this range. In contrast the band pass filter passes all frequencies within a frequency range of f_1 and f_2 stops all other frequencies outside of this range [20].

In this present research work, authors main focus is on the high pass filter so it has been elaborates. A high pass filter is an electric filter that passes signals with a frequency higher than a certain cut-off frequency. The gain of high pass filter increases at a constant rate of *20 db/decade* (first order). The gain reaches a constant value (A_{max}) as frequency increases and exceeds a certain limit. The cut-off frequency yields a gain that is given by $0.7071 \times A_{max}$. [21-23]. The cut-off frequency for an ideal first order filter is given by:

$$f_c = \frac{1}{2\pi RC} \tag{1}$$

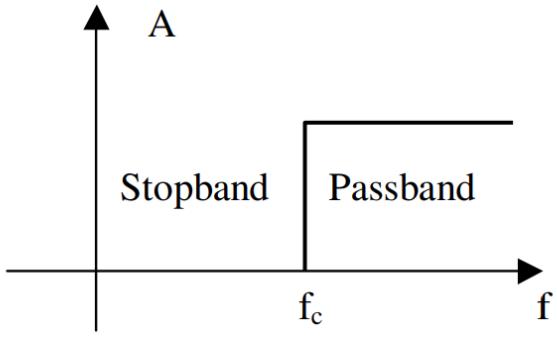


Figure 1. Ideal high pass filter response [10].

The ref. [24] has the design of third order HPF by cascading a typical first order and second order active filter. However, now the core of the circuit (op-amps) was replaced with folded cascode op-amp (which utilizes MOSFET Technology) with a cut-off frequency of *1 GHz*. An op-amp is added to this designed structure of high order filters as it allows the filter to have gain. Higher filter order results in enhanced filtering effect. The folded cascade op-amp in [25, 26] was designed with miller capacitor compensation. Therefore, this present work will follow a similar principle however the op-amps in the filter will be designed using two-stage CMOS topology and a nulling zero in series with compensation capacitor for compensation strategy as research has shown this results a better PSRR, unity gain bandwidth, CMRR and lower power dissipation [27-29].

Table 1. Op-amp design specifications

Design parameters	Design Specifications	CMOS
V_{DD}	5V	5V
V_{SS}	-5V	-5V
Open loop DC gain	> 50 dB	57 dB
Unity gain bandwidth	> 1 MHz	≈ 50 MHz
Slew rate	> 2 V/μs	--
CMRR (dB)	> 80 dB	--
Phase margin	$\approx 45^0$	$\approx 42^0$
Load capacitance	1.5pF	1.5pF
Power dissipation	< 1W	--

According to these design specifications the most suitable op-amp topology and op-amp compensation was chosen to be utilized in this design.

In this work authors have design an analogue filter that will be applied with an RF switch in a transceiver system. It implements CMOS technology to eliminate the need for conventional op-amps with low gain and high power consumption. This filter has low insertion and operating losses, eliminate low frequency components of the input signal. At later sections it has been compare with the existing conventional filters (which uses active

devices such as OP-AMPs with BJTs) to determine if the designed filter transfer function and frequency response is obtained. The designed high pass filter can be applied together with RF switch in transceiver system. The work presented in the paper is as follows: Section 2 describes the basics of 3rd order filter. Section 3 details the Ideal CMOS op-amp component analysis. The Simulation results with Conventional filter has been explained in Section 4 which will be used as a comparative model. Section 5 has the CMOS op-amp based design, and Section 6 has the fabricated model of 3rd order HPF with two-stage CMOS op-amp. The Section 7 has result and analysis with discussions. Finally, conclusion of the work and future perspectives are detailed in the Section 8.

2. Basic concept for System Design of 3rd Order HP Filter

To design a third-order unity gain Bessel high pass filter with the corner frequency of 1 kHz, the coefficients for a third order Bessel filter is obtained from [30, 31]:

Table 1. Bessel filter coefficients

Order number (n)	Filter number	a_i	b_i
3	Filter 1	a_1=0.756	b_1=0
	Filter 2	a_2=0.9996	b_2=0.4772

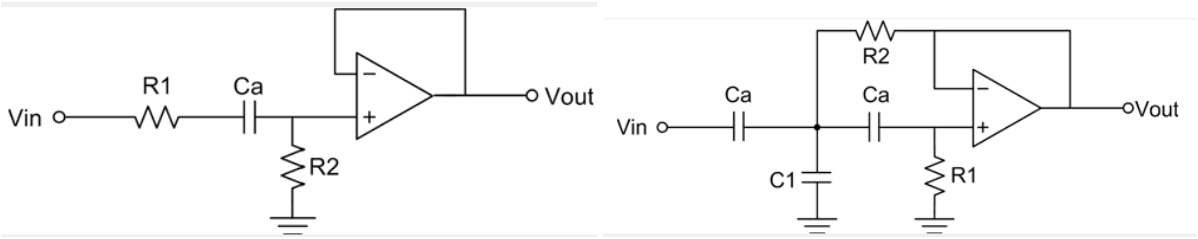


Figure 2. First and Second order filter.

A. *First order filter*

Since the design requires that gain is *1*, hence $R_1 = R_{sig}$. Assume $C_a = 10\ nF$, therefore, using Eq. (1):

$$R_2 = \frac{1}{2\pi f_c a_1 C_a} = \frac{1}{2\pi\left(10^3\right)\left(0.756\right)\left(10\times10^{-9}\right)} = 21.5k\Omega \tag{2}$$

The parameters of the first stage transfer function were obtained from the analogue filter design toolbox [32].

$$T\left(S\right) = \frac{ks}{s-p} \tag{3}$$

where $Z = 0$, $p = -4750.4$, $k = 1$, $\omega_o = 4750.36$, and $\omega_z = 0$. The sensitivity of the first stage parameters to the variation in component values was determined from the analogue filter design toolbox. This gave an indication of how a slight variation in component values can change the filters parameters.

Table 2. Sensitivity analysis

	Stage 1			Stage 2		
	ω_o	**|ρ|**	**Q**	**ω_o**	**|ρ|**	**Q**
C_a	-0.9901	-0.9901	-1.6066e-14	-0.9901	-0.9901	-1.6066e-14
R_1	-0.49628	-0.49628	0.49876	-0.49628	-0.49628	0.49876
R_2	-0.9901	-0.49628	-0.49628	-0.49628	-0.49628	-0.49628

B. Second order filter

Assume C_a = C_a = *10 nF*,

$$R_1 = \frac{1}{\pi f_c C(a_2)} = \frac{1}{\pi\left(10^3\right)\left(10\times10^{-9}\right)\left(0.9996\right)} = 31.8k\Omega$$

Closest 1206 SMD value available is *33 k*Ω.

$$R_2 = \frac{a_2}{4\pi f_c C b_2} = \frac{0.9996}{4\pi\left(10^3\right)\left(10\times10^{-9}\right)\left(0.4772\right)} = 16.7k\Omega$$

Closest 1206 SMD value available is 15 *k*Ω and Transfer function will be:

$$T(s) = \frac{ks^2}{(s-p)\left(s-p^*\right)} = \frac{ks^2}{s^2 + s\left(\frac{\omega_0}{Q}\right) + \omega_o^2} \tag{4}$$

Where Z = 0, p = -3140.4±j2996.1, k = 1, ω_o = 4340.4, and ω_z = 0, Q = 0.69105. As in stage 1, the sensitivity analysis of the second stage parameters were obtained from the analogue design toolbox.

C. Overall third order ideal filter design

The overall transfer function of an ideal third order unity gain Bessel filter will be in format of [33, 34]:

$$T(S) = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \tag{5}$$

Where a_0, a_1, and a_2 are *0*, and b_0*=8.94909e+10*, b_1*=4.86751e+07*, b_2*=11031.2*, and a_3 and b_3 are 1. Alternatively,

$$T(s) = \frac{k(s-z_1)(s-z_2)(s-z_3)}{(s-p_1)(s-p_2)(s-p_3)} \tag{6}$$

Where *k* = 1 and, Z_1, Z_2, and Z_3 are 0, and p_1 = -3140.43-j(2996.08), p_2 = -3140.43+j2996.08, and p_3 = -4750.36. The poles and zeroes were plotted as shown in the diagram below for a third order high pass Bessel filter with a cut off frequency of 1 kHz. The filter has three poles and zero at the positions as indicated in Table 3 and Fig. 3. The frequency of the input at the filter was varied to determine the magnitude and phase of the ideal filter's transfer function.
The frequency response plot of the ideal third order high pass filter was then obtained and it can be seen that the cut-off frequency of *1 kHz* occurs at a gain of *-3 dB* as desired is shown in Fig. 4.

Table 3. Frequency response of ideal filter

Frequency	Magnitude	Phase
1 Hz	2.7717e-09=-171.145dB	$-90.1958^0 = -1.57421 rads$
5 Hz	3.465e-07=-129.2dB	$-90.98^0 = -1.588 rads$
1 kHz	0.7071=-3.01dB	$99.48^0 = 1.736 rads$
2 kHz	0.923716=-0.689232dB	$= 50.2834^0 = 0.877611 rads$
5 MHz	1=-1.071e-07	$0.02012^0 = 0.0003511 rads$

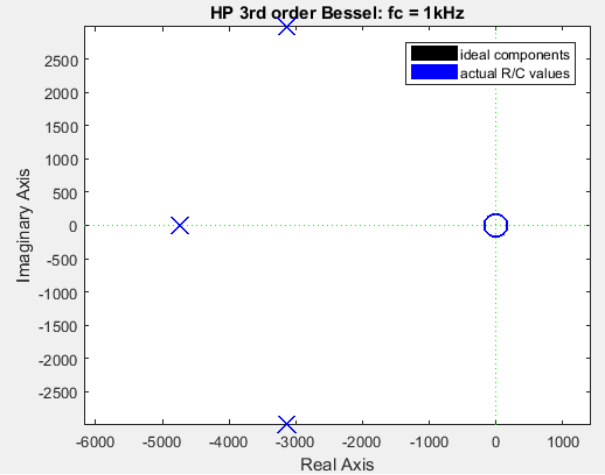


Figure 3. Pole and zero diagram of ideal Bessel third order high pass filter.

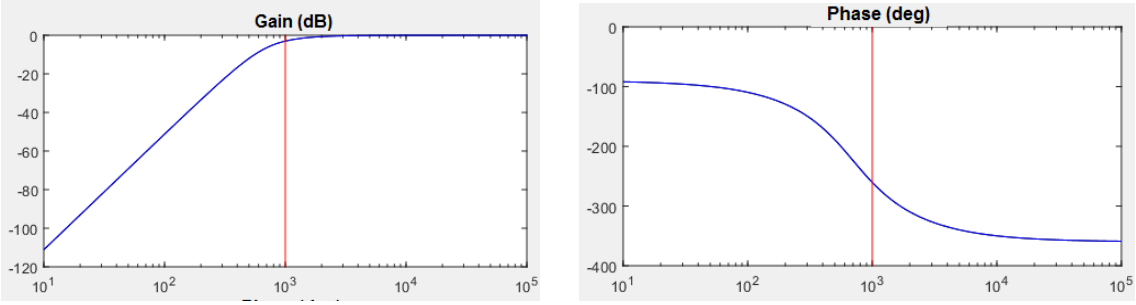


Figure 4. Frequency response of ideal third order high pass filter.

3. CMOS op-amp component analysis

The parameters of ideal CMOS op-amp have been calculated and the bias current was determined, so that the appropriate component values could be used in the circuit schematic [35-40]. For the model of Fig. 5 the mathematical analysis is as follows: ()

$$Vx = V_t V_{TON} \tag{7}$$

Where Vx is nodal voltage, VTON is turn-on voltage and Vt is threshold voltage. The unity gain Bandwidth:

$$UGBW \approx \frac{\left(-\frac{g_{m_{N1}}}{C_c}\right)}{2\pi} \tag{8}$$

Assume $UGBW = 100MHz$ and $g_{mN1} = 1ms$

$$C_C = \frac{g_{mN1}}{2\pi(100M)} = 1.6\,pF \tag{9}$$

Closest available 1206 SMD Capacitor is 1.5pF

$$P_2 = -\frac{g_{MP3}}{2\pi C_L} \tag{10}$$

Assume the second pole introduced by the op-amp is at *200 MHz* and load capacitor (C_L) = *1.5 pF* (1206 SMD capacitor used), Transconductance $g_{MP3} = 2\pi C_L P_2 = 1.88ms$. Assume the second pole and zero overlap at *200 MHz* (far away from the filters operating bandwidth of frequencies):

$$P_2 \approx Z \tag{11}$$

$$\Rightarrow Z = -\frac{1}{\left(R_z - \frac{1}{g_{MP3}}\right)C_C} \tag{12}$$

Where C_c is the compensation capacitor, z and P are the zero and pose respectively.

$$R_Z = \left(1 + \frac{C_L}{C_C}\right)\left(\frac{1}{g_{MP3}}\right) = 1063.83\Omega$$

Closest available 1206 SMD Resistor is *1.2 kΩ*.Also,

$$g_{MN1} = g_{MN2} = 1ms \tag{13}$$

$$g_{MN1} = \frac{2I_{bias}}{V_{TON}}$$

$$I_{bias} = \frac{1}{2}(g_{MN1})(V_{ON}) \tag{14}$$

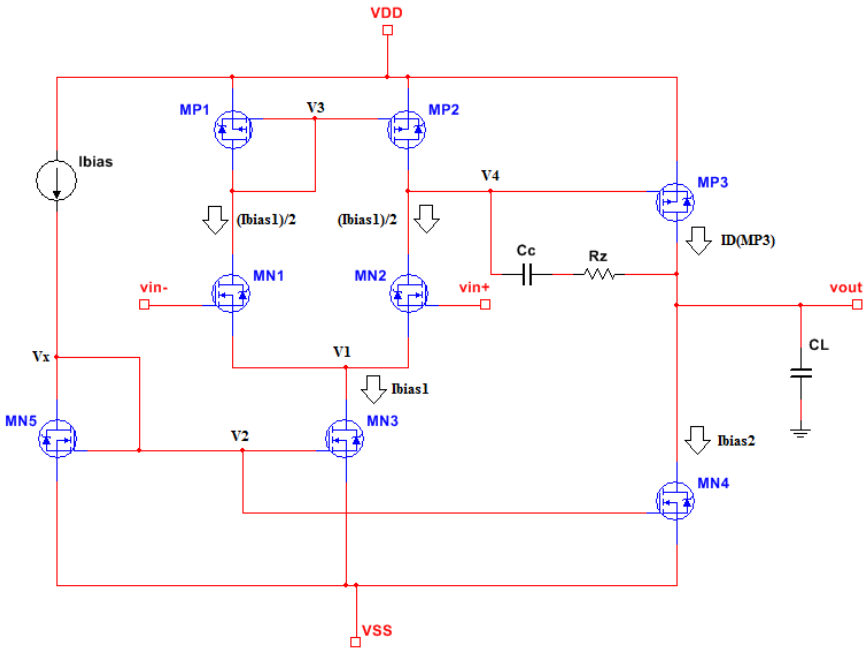


Figure 5. Ideal Two-stage CMOS op-amp [40]

Assume V_{ON} and $|V_T|$ is the same for both N-MOS and P-MOS as they are complementary.

$$I_{DS} = k_{p,n}{}'\left(\frac{W}{2L}\right)V_{ON(n,p)}^2 \tag{15}$$

$$\left(\frac{W}{L}\right)_{MN1} = \left(\frac{W}{L}\right)_{MN2} = \frac{2I_{DS}}{k'V_{ON}^2}$$

$$I_{bias1} = 2 \times I_{bias} \tag{16}$$

This Eq. (16) does not apply to real applications as the width and length of commercial MOSFETs are generally $W = 100\ \mu m$, $L = 100\ \mu m$, or $W = 1\ \mu m$, $L = 1\ \mu m$, as stated in the spice model of the manufacturer [41-44]. Therefore,

$$I_{bias1} \approx I_{bias} \tag{17}$$

$$\left(\frac{W}{L}\right)_{MN3} = \frac{2I_{DS(MN3)}}{k'V_{ON}^2} = 2\left(\frac{W}{L}\right)_{MN1}$$

$$\left(\frac{W}{L}\right)_{MP1} = \left(\frac{W}{L}\right)_{MP2} = \frac{2I_{DS(MP2)}}{k'V_{ON}^2} \tag{18}$$

Bias current of second stage:

$$g_{MP3} = \frac{2I_{DS(MP3)}}{V_{ON}} \tag{19}$$

$$I_{bias2} = I_{DS(MP3)} = \frac{g_{MP3}(V_{ON})}{2}$$

$$\left(\frac{W}{L}\right)_{MP3} = \frac{2I_{DS(MP3)}}{k_p'V_{ON}^2} \tag{20}$$

4. Simulation results with Conventional filter

The third order high-pass filter with the calculated component values has been simulated with Multisim using general all purpose LM741 op-amps as shown in Fig. 6. This was done to form a comparison of the conventional filter with the designed filter. The magnitude and phase plot, and the transient response of the conventional filter has been analysed.

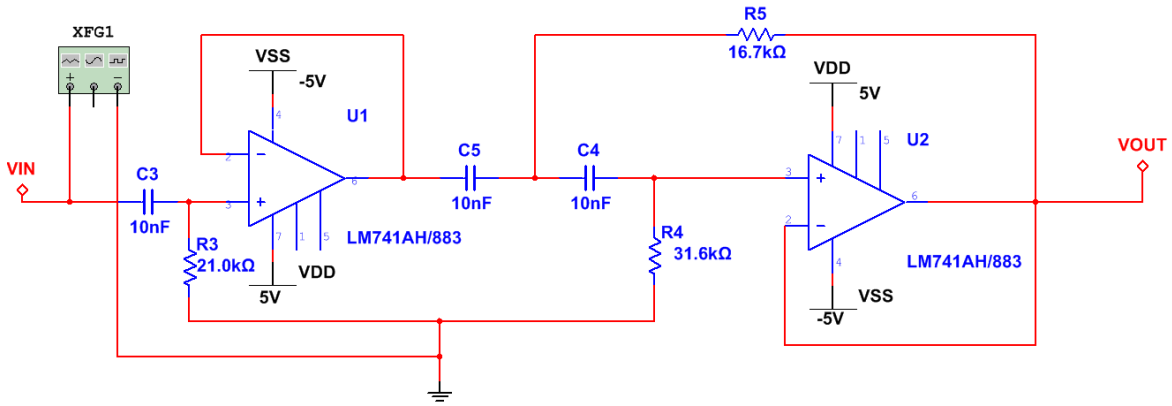


Figure 6. Conventional filter used for comparison.

The gain of the conventional filter's bode plot drops from *0 dB* at around *600 kHz* (Fig. 7, and Fig. 8), indicating this filter has a smaller bandwidth. The phase response of the conventional filter was obtained and is as expected for a Bessel filter. The input frequency of the conventional filter was varied and transient response of the input (blue) and output (red) was observed. It can be seen that the bandwidth operation of the conventional filter is around *300 kHz* until the gain starts to drop and the output becomes attenuated as shown in Fig. 10.

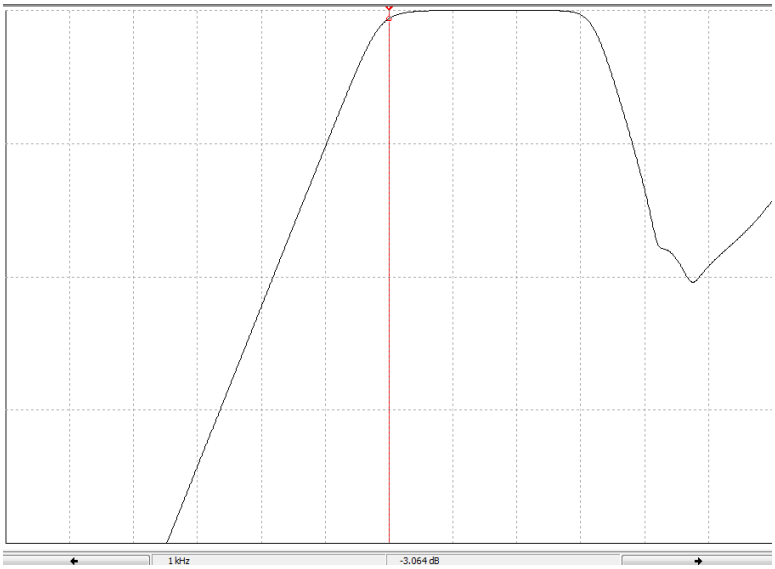


Figure 7. Magnitude bode plot of a conventional third order high pass filter

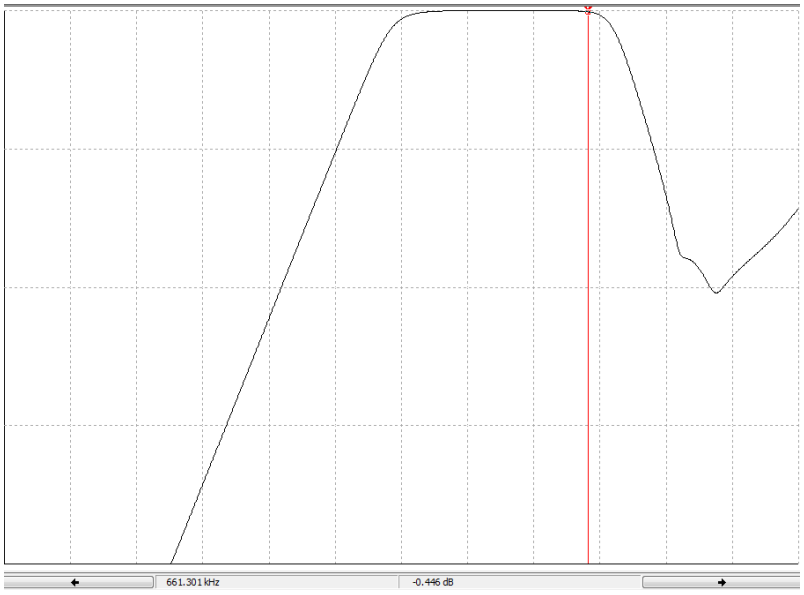


Figure 8. The bode plot starts to decrease at 600kHz

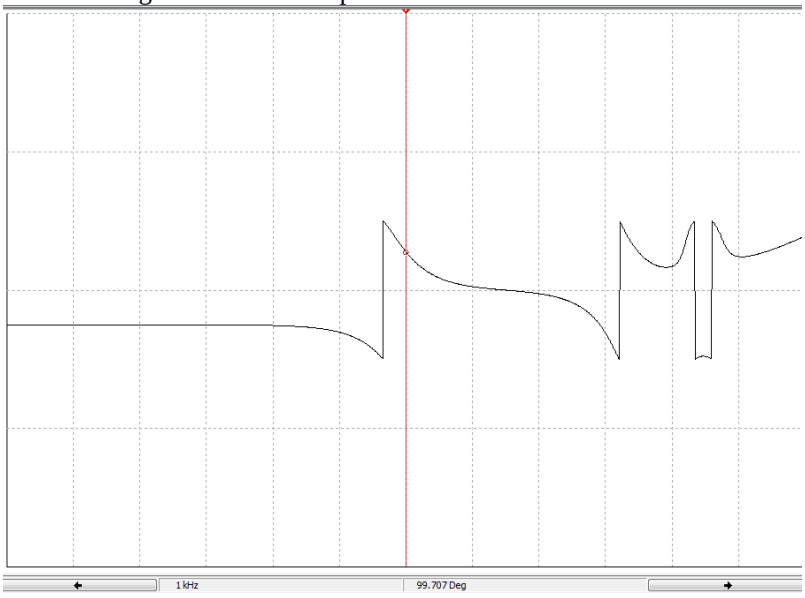


Figure 9. The phase response of the conventional filter

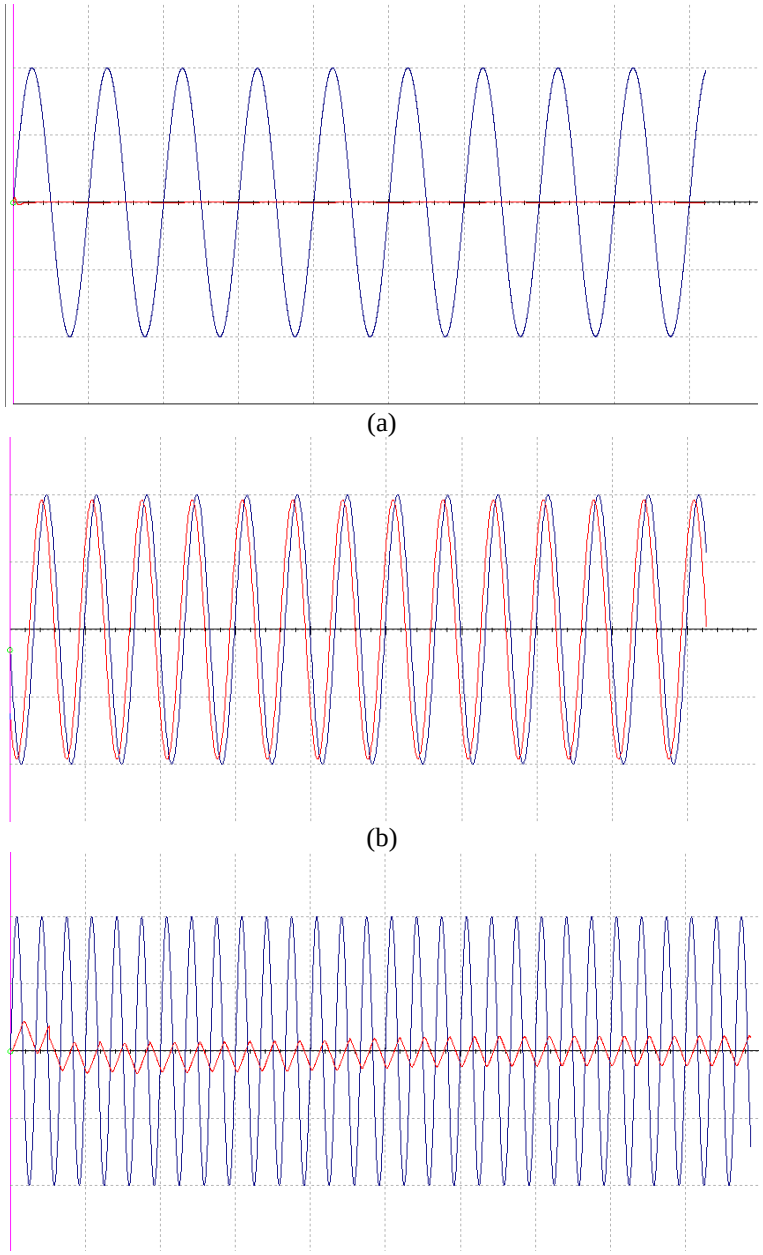


Figure 10. Transient response of the conventional filter at (a) 100 Hz, (b) 3 kHz, and (c) 300 kHz

5. Proposed CMOS op-amp design

The two-stage CMOS op-amp has been connected with the first stage differential amplifier made up of an n-MOS differential pair input (MN_1 and MN_2) and p-MOS active loads (MP_1 and MP_2). The configuration allows for dual-input and single-ended output to the second stage. The second stage comprises of an inverting p-MOS amplifier (MP_3) and an n-MOS bias transistor which ensures the output has approximately zero dc current. The bias circuitry which consists of R_4, MN_5, MN_3 and MN_4 has been used to ensure that all transistors operate in the saturated region. Transistors MN_5 and MN_3 act as current mirrors providing the bias current at the differential amplifier. Transistors MN4 mimic the current of the bias circuitry. Transistors MP_1 and MP_2 acts as active load and are complementary to MN_1 and MN_2 with similar threshold voltage to ensure the current in each branch is equal and half the bias current of the current mirror source. The capacitor C_2 serves as a compensation capacitor to prevent the op-amp when used in inverting feedback from reverting to positive

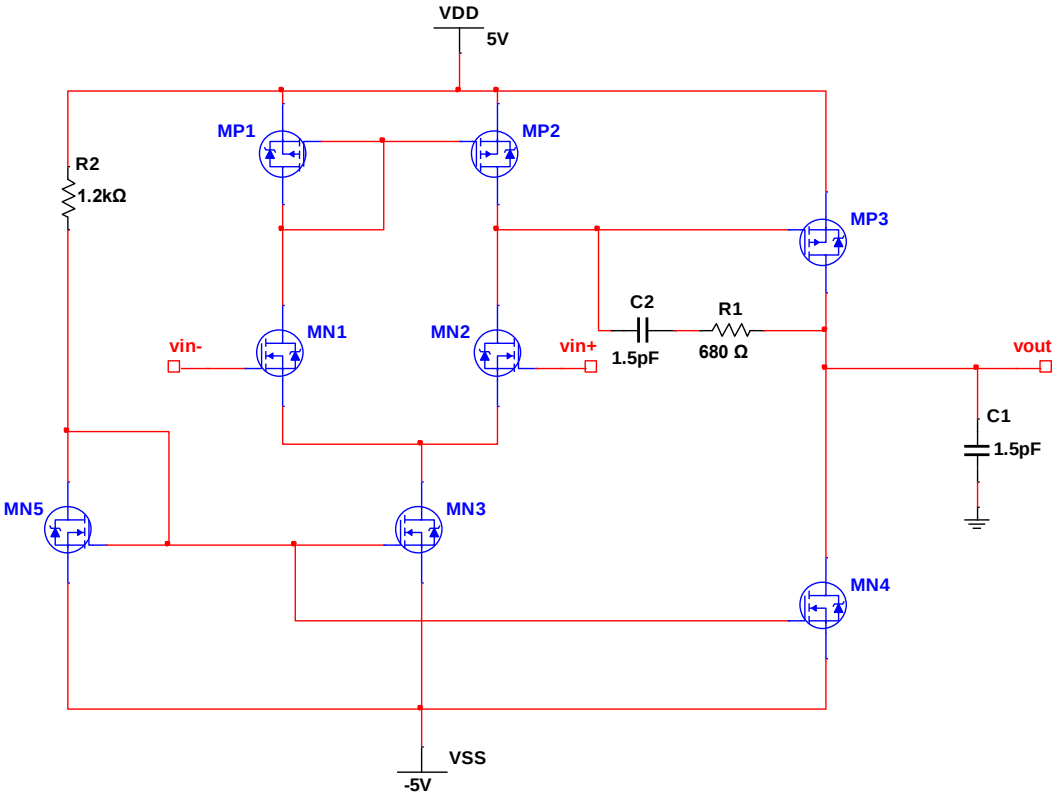


Figure 11. Two stage CMOS op-amp schematic.

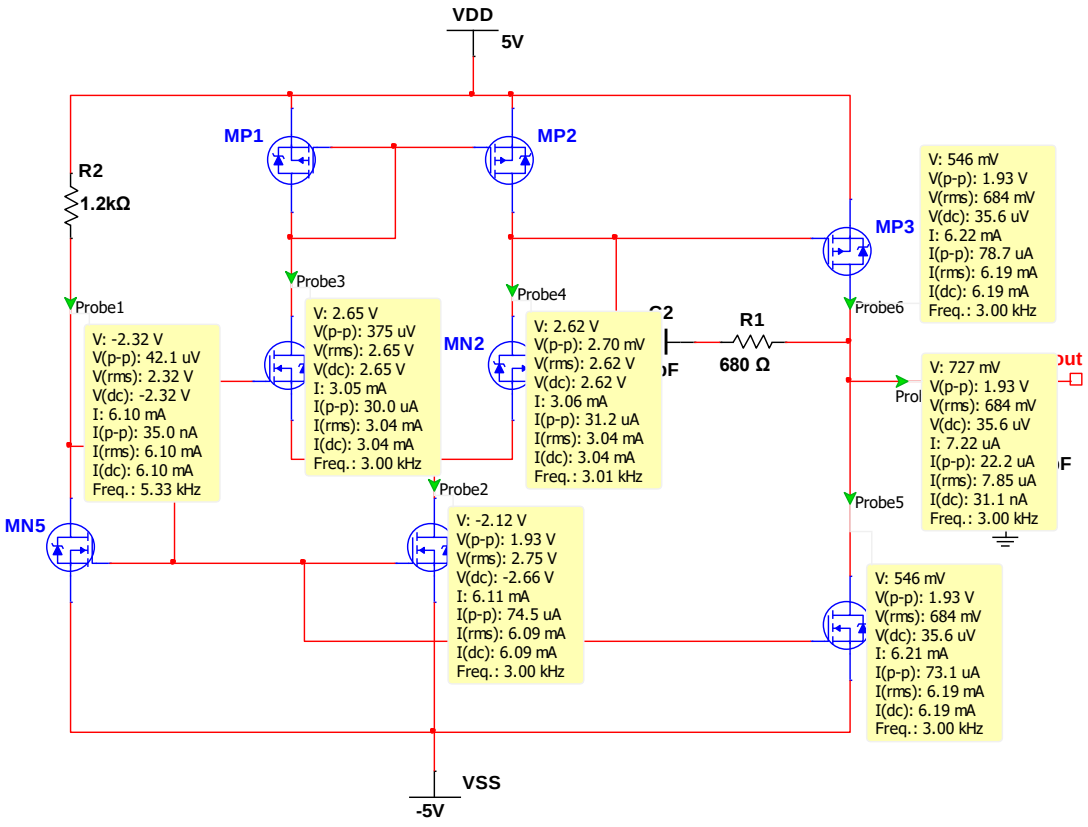


Figure 12. DC Nodal Analysis of Two stage CMOS op-amp schematic.

feedback due to 180^o phase shift that is caused by the two poles introduced from the CMOS op-amp. The capacitor C_2 splits the poles and pushes the second pole beyond the unity gain

bandwidth of the designed op-amp. The resistance R_1 is used as nulling resistor for frequency compensation as it eliminates the right half plane zero that the two stage CMOS op-amp introduces. The capacitor C_1 serves as the capacitive load of the op-amp at the output.

A. DC Nodal Analysis

A dc nodal analysis has been performed at the branches of the two-stage CMOS op-amp to determine if the bias circuitry is correct and the transistors are in saturation region. The bias current is *6.10 mA* and the output drain current of the current mirror is *6.11 mA* which is approximately the same. The drain current in the branches of the active load are approximately half of the bias current which is as expected. The current at the output node is *7.22 μA* which is really small and negligible. These current and voltage at each node and branch is subject to change with the variation of MOSFET component selection and the power supply utilized. The MOSFETs chosen for simulation are complementary in nature with the same threshold voltage.

B. Overall filter design

The two-stage CMOS op-amp has been designed and analyzed, thereafter a hierarchical block was created in Multisim to replace one of the LM741 op-amps with the designed two stage CMOS op-amp to determine the improvements to the overall filter response as shown in Fig. 13. The two-stage CMOS op-amp is used in the second stage of filter (second order) and is connected in a unity gain negative feedback configuration shown in Fig. 14. The filter has been connected according to the system design calculations and should operate at a cut-off frequency of *1 kHz*.

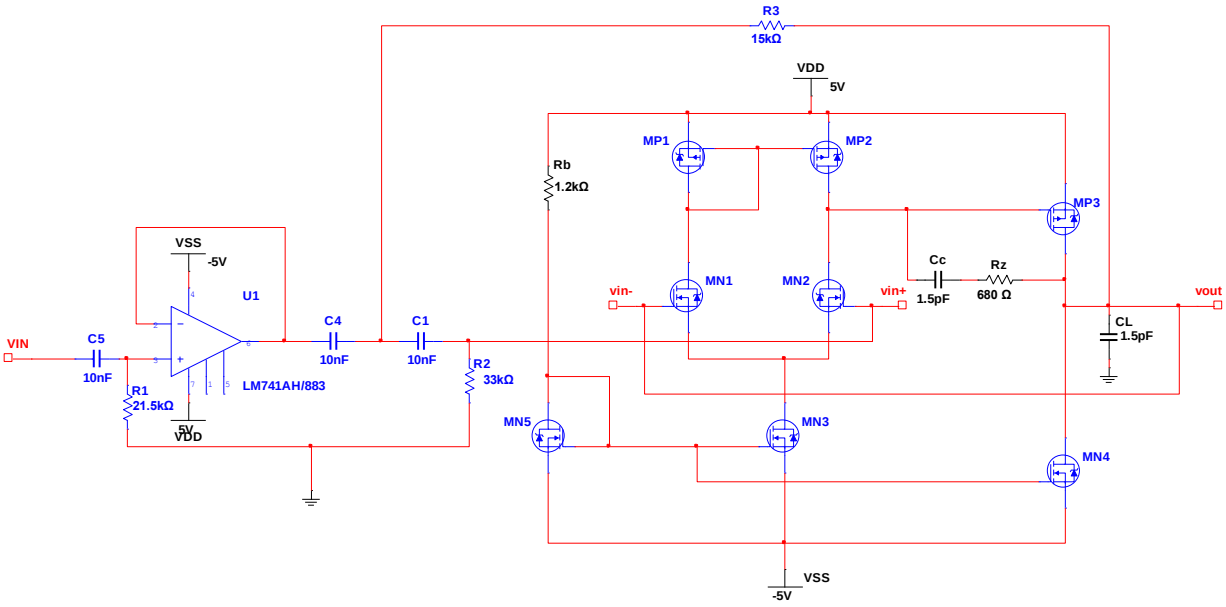


Figure 13. Overall circuit of designed third order high pass filter.

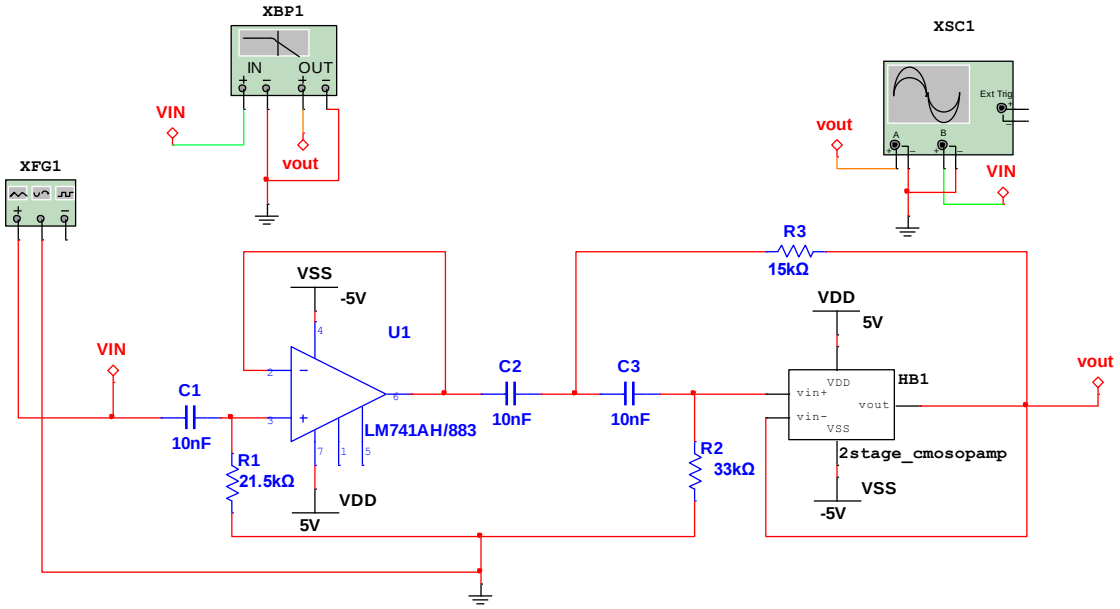


Figure 14. Simplified Overall circuit of designed third order high pass filter for testing.

C. AC Response

The frequency and phase response was simulated and analysed in Multisim as displayed in Fig. 15. The responses are close to that of the ideal filter which was simulated in MATLAB.

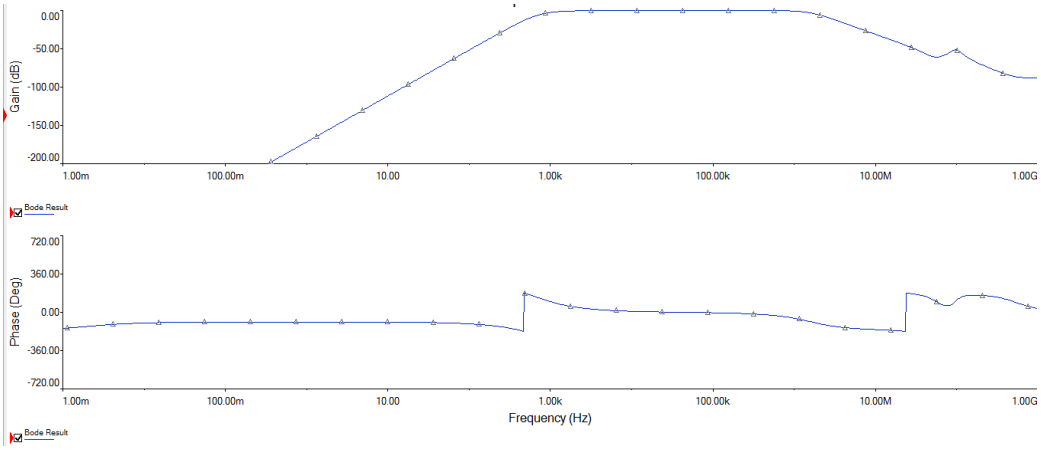


Figure 15. Frequency and phase response of designed filter.

The bode plotter feature from Multisim has been utilized to determine the gain and phase of the designed filter at different frequencies. The cut-off frequency of the designed filter is *1 kHz* at gain -2.58 dB as shown in Fig. 16. The maximum passband gain of the designed filter as shown in Fig. 17 is 0 dB, which is as calculated. The gain of the designed filter begins to decrease at around 1 MHz which is shown in Fig. 18. This indicates that the designed filter has a better frequency response than the conventional high-pass filter.

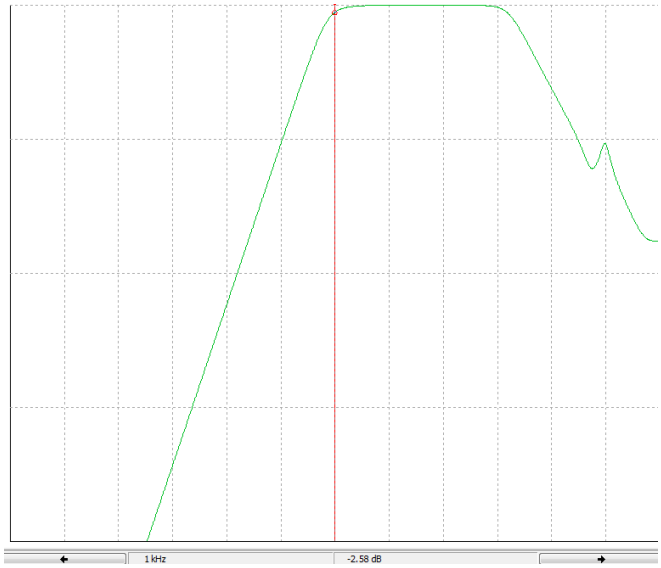


Figure 16. Cut-off frequency of the designed filter

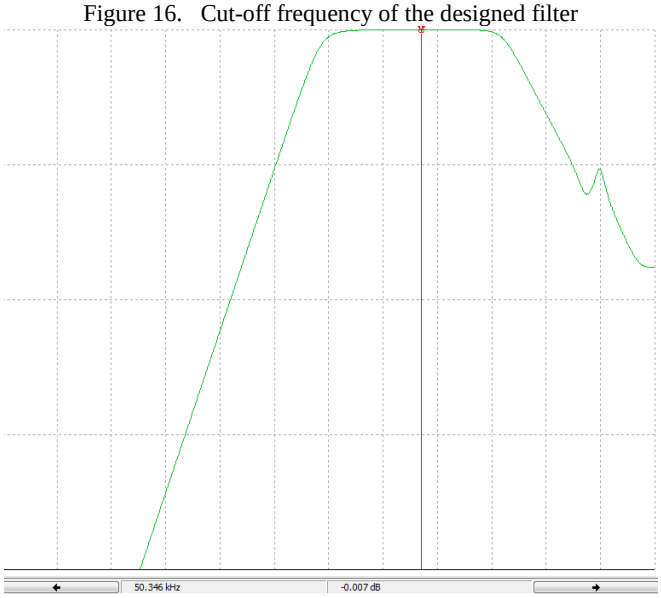


Figure 17. The passband gain of the designed filter

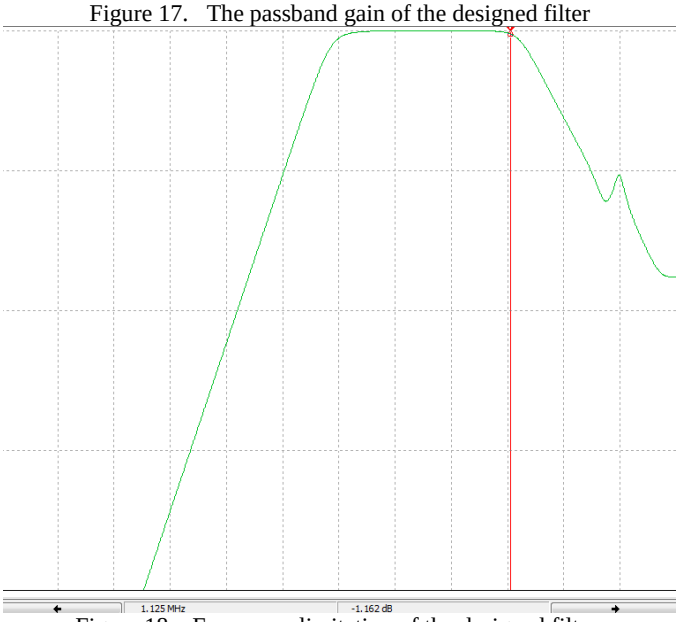
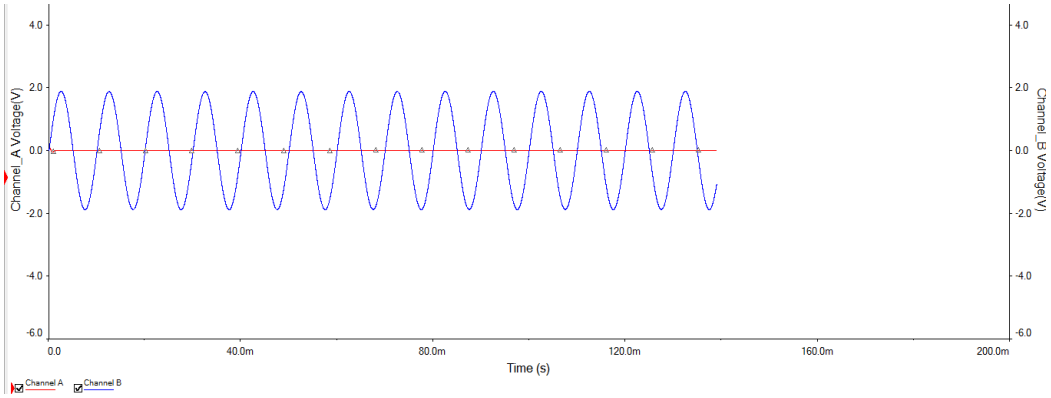


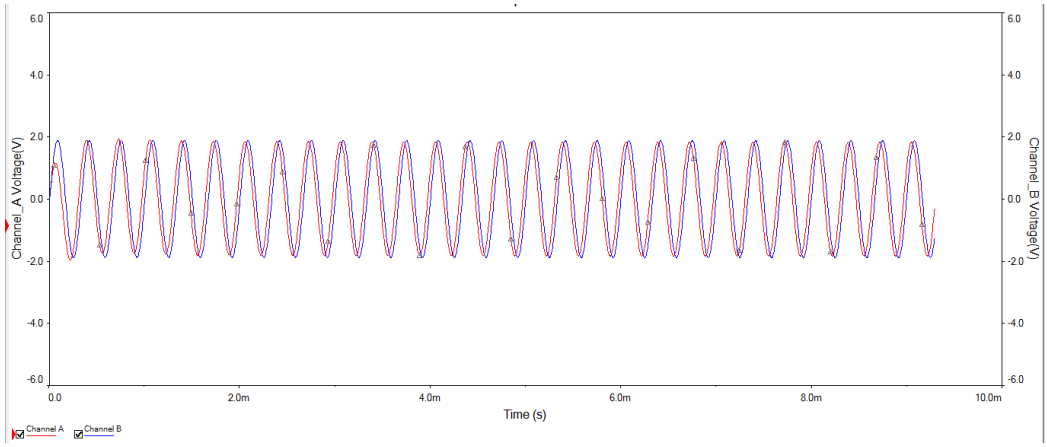
Figure 18. Frequency limitation of the designed filter.

D. Transient response

The transient response of the designed filter has been analysed with an input (blue) signal at 100 Hz, 3 KHz, and 2 MHz as shown in Fig. 19. The volts/div was kept the same for both channels. It can be seen that the output (red) has been attenuated at 100 Hz. This indicates that the designed filter has good frequency response.



(a)



(b)

Figure 19. Transient response of the designed filter at (a) 100 Hz, and (b) 3 kHz.

For an input signal of *2 MHz*, it can be seen that the output (red) signal has amplitude which is lower than the input (blue) signal. The output signal is also rather noisy; this is due to the effect of the parasitic capacitance in the MOSFETS which increases rapidly at around 1 MHz (stipulated in MOSFET datasheets) as shown in Fig. 20.

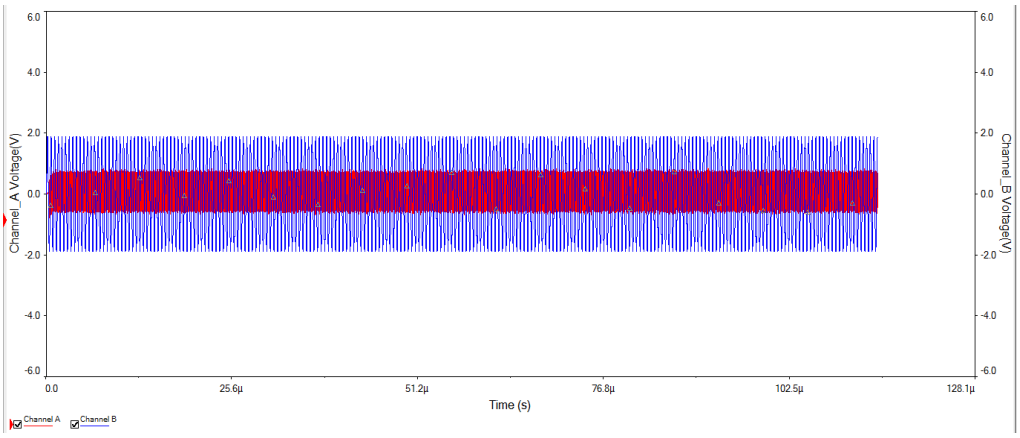


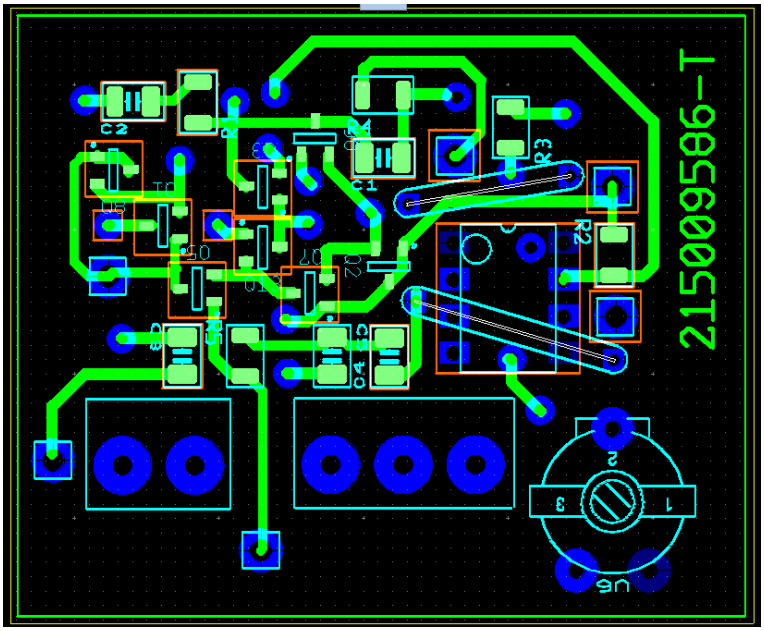
Figure 20. Transient response of designed filter above frequency limitation.

6. Fabrication of 3rd order HPF with two-stage CMOS op-amp

The process of finding the suitable MOSFETs is a cumbersome process. Therefore, various manufacturer datasheets have been analysed to find n-channel and p-channel MOSFETs with similar threshold voltages to ensure that all MOSFETs would operate in the saturation region with the designed bias circuitry to give the desired op-amp behaviour. The design objective is to fabricate a circuit with minimal chip area as these filters would be utilized in portable electronics devices [45-48]. Therefore, SMD SOT 23 package has been selected for all MOSFETs, as this matched the smallest allowed printed circuit rack size. Another important factor to consider is maximum rating of the MOSFETs to ensure that breakdown voltage is not reached, as this would cause leakage current and increases the power consumption (even the device is not in use) due to thermal heating. A power supply of 10 V is being utilized to power the filter's op-amps therefore MOSFETs with a maximum V_{ds} of 50 V has been selected.

The resistors and capacitors chosen are vital to ensure the closest desired filter response is achieved. The filter parameters sensitivity to component variation has been calculated in Table 2. The electrical rating has also considered when choosing these components, therefore components rated at 50V, 0.25W, 1% tolerance has been selected to ensure optimum and safe response.

A circuit board has been created to test the behaviour of designed third order high-pass filter. This circuit has been implemented on double-sided printed circuit board as opposed to Vero board or breadboard to reduce the effects of noise from jumper cables or loose connections.



(a)

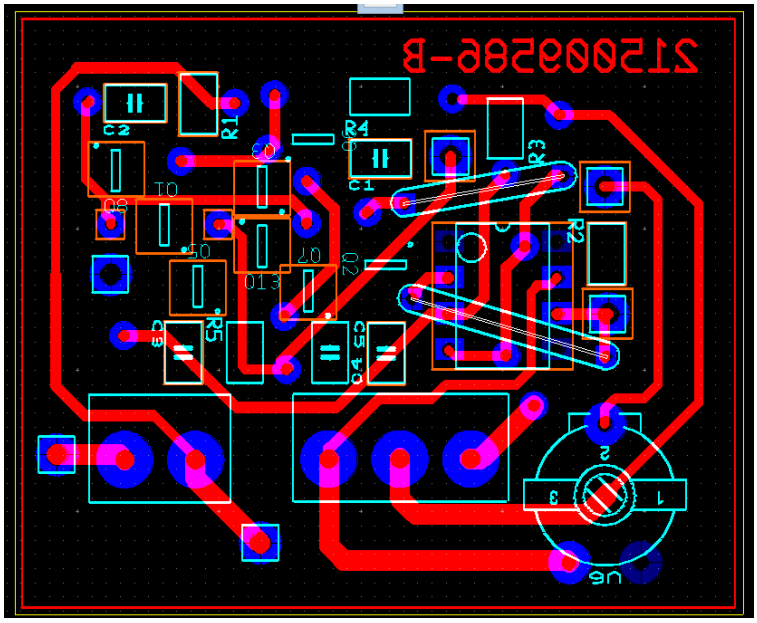


Figure 21. Designed 3rd order high pass filter with two stage CMOS op-amp (a) top view and (b) bottom view.

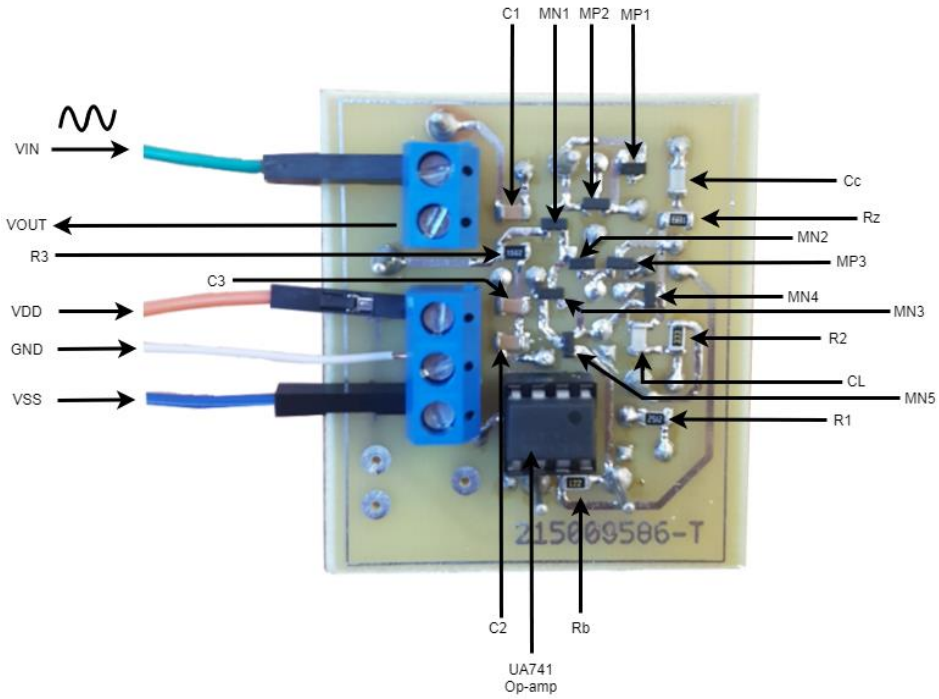


Figure 22. Fabricated 3rd order HPF with two-stage CMOS op-amp.

The filter implemented has been powered with a LODESTAR LS-1330 triple output DC power supply for testing purposes. This supply allowed for ± 5 V and current rating of 0 A to 3 A. An FG601 function generator has been utilized to provide a sinusoidal input to the filter of 1Vp-p with the frequency being varied to observe the transient response of the filter.

The third order filter high pass filter with designed two-stage CMOS op-amp has been implemented is shown in Fig 22. There are several test points added to the circuit to test the behaviour of the high pass filter at different nodes.

The components utilized and soldered on the double-sided printed circuit board are: MN_1, MN_2, MN_3, MN_4, MN_5 - BSS138 or 2N7002 N-channel MOSFET, MP_1, MP_2, MP_3 - BSS84 P-channel MOSFET, R_1 = 21.5 kΩ, R_2 = 33 kΩ, R_3 = 15 kΩ, R_z = 680 Ω, R_b = 1.2 kΩ, C_1, C_2, C_3 are 10 nF, and C_c, C_L are 1.5 pF.

7. Result and Analysis with Discussions

The transient response of the third order high pass filter with designed two-stage CMOS op-amp has been analysed and it can be observed that the gain is approximately *-3 dB* at *1 kHz* as shown in Fig. 23(b). Here V_{OUT} (blue) is connected to channel 1 and V_{IN} (red) is connected to channel 2.

For 30 kHz, the gain is approximately *0 dB* at as shown in Fig.23(c). Here V_{OUT} (yellow) is connected to channel 1 and V_{IN} (blue) is connected to channel 2. The output has the same amplitude as the input signal at *30 kHz* (above cut-off frequency), this implies the designed circuit has good filtering effect.

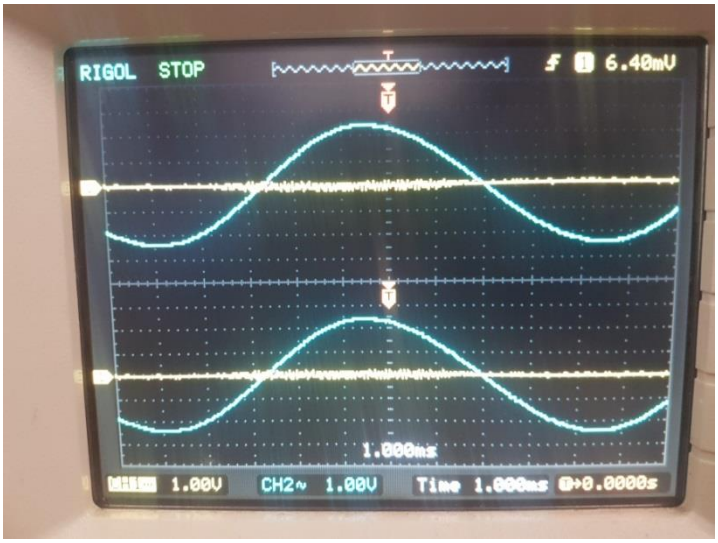
Also, it can be observed from Fig. 23(a) that the gain really low at *100 Hz, w*here V_{OUT} (yellow) is connected to channel 1 and V_{IN} (blue) is connected to channel 2. The output has a very small amplitude (almost completely attenuated) compared to the input signal at *100 Hz* (below cut-off frequency), this implies the designed circuit has good filtering effect.

The current at the supply branches were measured to determine the overall power consumption of the designed filter.

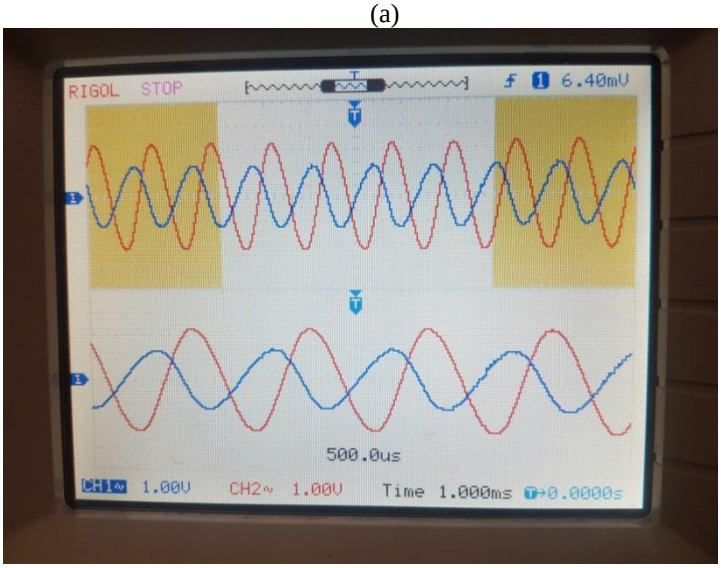
$$\begin{aligned} P_t &= P_n + P_p \\ &= VnI_n + V_pI_p \\ &= (-5)(-25m) + 5(25m) = 0.25W \end{aligned} \tag{21}$$

The results obtained from the hardware implementation of the designed third order high pass filter correlated to that of the simulated results of the filter. When the input signal of the filter is set at a frequency below cut-off frequency, the output is attenuated. However, if input signal of the filter is set to above the cut-off frequency, the output has the same amplitude as of the input signal indicating that the designed filter has good filtering effect. The transient response has been physically observed for different types of MOSFETs to determine which type will provide the desired filter response. It has been noticed that small signal MOSFET transistors operated better in this circuit schematic as opposed to power HEXFET MOSFETs [49-51]. The use of HEXFET power MOSFETs rated at a maximum V_{DS} of 30 V caused the output signal to slow down and affected the amplitude of the output signal at very high frequencies. The designed circuit has a small chip area as the components selected were SMD and SOT-23 package. The use of double-sided printed board helps to reduce noise that would have been brought about by jumper wires. It has been noticed that the use of CMOS op-amp in the filter design allowed the filter to operate at faster speeds.

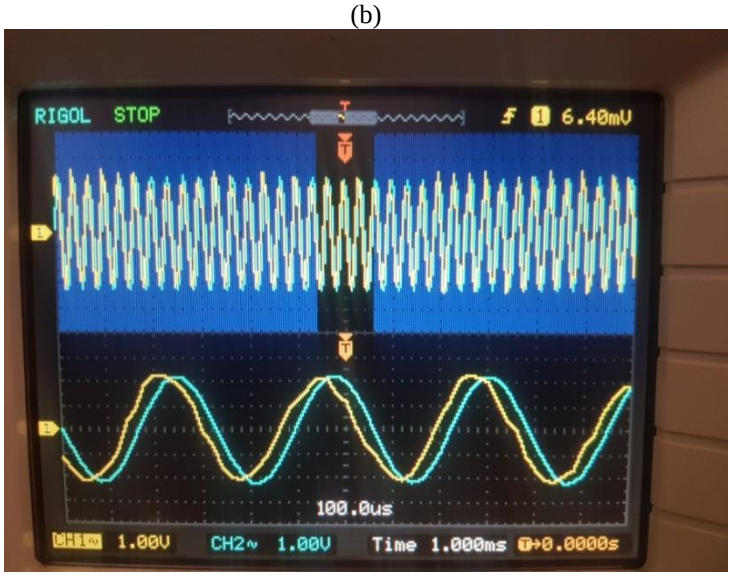
The use of small signal MOSFETs allowed the use of a scaled down supply voltage of ± 5V, this supply voltage has been chosen as the minimum supply voltage for the first stage is also ± 5V. The transient response of the filter with the design two stage CMOS op-amp has been compared to the filter with commercial CMOS op-amp and it has been analyzed that the transient response obtained are very similar when the frequency is varied. This indicates that the designed CMOS op-amp has the desired high input impedance and low output impedance behaviour as commercial op-amps possess and has a similar frequency bandwidth.



(a)



(b)



(c)

Figure 23. Transient response of designed filter at (a) 100 Hz, (b) 1kHz, and (c) 30 kHz

Table 4. Overall filter parameters

Parameter	This work
Power supply	± 5V
Filter order	N = 3
Filter type	Unity gain Bessel filter
Cut-off frequency	1 kHz
Q factor	0.69105
Power consumption	0.25 W
Maximum pass band gain	0 dB
Circuit area size	52x47 mm

By replacing just one of the LM741 op-amps with two stage CMOS op-amp, this resulted in the bandwidth of the overall filter to increase from *600 kHz* to *1 MHz*. The chip area of the filter would also be further reduced. The cut-off frequency and bandwidth of the filter can be changed to higher frequency ranges by simply adjusting the calculations.

8. Conclusions and Future Recommendations

An extensive research analysis has been undertaken to determine existing filter designs. The use of CMOS op-amps in filter design is suitable and justified due to the reduced power consumption and enhanced dc gain, CMRR, Slew rate, unity gain bandwidth, etc. compared to conventional op-amps utilized. The designed circuit is suitable for high frequency, wireless and satellite communication systems. The development with CMOS technology has resulted in the realization of circuits with reduced chip area. The implemented and designed third order high pass filter with two stage op-amp on hardware is functioning as expected according to the simulated results. The transient response of the input and output signals was measured to determine if the output was varying with a change in input frequency. The output maintained the same amplitude as the input signal above cut off frequency and attenuated signals below cut off frequency indicating that the filter displays good filtering effect.

A recommendation is to replace the LM741 op-amp in the first stage with a simple MOSFET differential amplifier as this would reduce the power consumption of the overall filter.

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