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Research paper

Design and Implementation of High Speed and Low Power Factorial Circuit

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Abstract

This paper deals with design of factorial circuit which turns on only for valid inputs and thus reduce unwanted transitions in the parallel circuitry by switching off the unused multipliers for inputs less than the maximal. The inputs are fed to the multiplier circuit through tristate buffers and control signals are produced using decoder. This in turn minimizes the dynamic power dissipation and reduces delay. The experimental evaluation of the proposed factorial circuit is done using simulation outputs and by comparing the performance parameters with prior designs in terms of power dissipation and delay. The functionality of the proposed circuit is verified by implementing in a combination and permutation circuit.

1. Introduction

The factorial calculation is important in ALUs and MAC designed for general and special purpose computers. The main applications where the factorial circuit find its prime importance are in Combinators, Permutators, Newton Raphson and Taylor series. Factorial circuits are the important elements of Spread spectrum base band processors used in satellite, military and low power spectral density applications.

The fore most components for hardware implementation of factorial calculation are incrementer, decrementer and efficient multipliers for successive multiplication. Recursive iterations in factorial computation increases hardware complexity and delay. As number of multiplications increases for large values of input, the switching power consumption also increases. So parallel algorithms for factorial computation are proposed by Saha et al[1].

The factorial of an input number is the product of all integers upto the number. This can be achieved either by decrementing the number in steps of one and finding the product of all or incrementing the value in steps of one upto the given number from one and finding the product of all. However the computation of factorial of a k bit number require ∑i=1 to i=k (2k/2i) multipliers and produces unwanted switching for input less than 2k.

The circuitry for factorial computation proposed by Saha et al is shown in Figure 1. The circuit is divided into stages where stage 1 performs multiplication of two consecutive numbers up to the input. Stage 2 performs multiplication of two consecutive outputs of stage 1. Stage 3 performs multiplication of two consecutive outputs of stage 2 and so on till the final product is achieved. For the case of 4 bit input, Saha et al's design requires 4 stages to obtain the final product. However for a k bit input the Saha et al's design produces unwanted transitions for input less than 2k and dissipates high dynamic power and increases delay.

2. Proposed factorial circuit

The circuit modules of the proposed factorial design are 0/1 detector, Decoder, Reconfigurable parallel multiplier etc., The proposed factorial design works on the principle of switching ON only the required multipliers upto the input. The unused multipliers in the design are switched OFF and thus it reduces unwanted transitions in the parallel circuitry which in turn reduces dynamic power dissipation. [5]

The input bits are passed to the 0/1 detector circuit which detects whether the input is zero or one. Since the factorial of zero and one equals 1, the 0/1 detector produces 1 output for the case of 0 and 1 input. The Ctrl output of the 0/1 detector is used as the select signal for the output multiplexer. One input for the multiplexer is the output bits of 0/1 detector and the other input is the output from parallel multiplier circuitry.

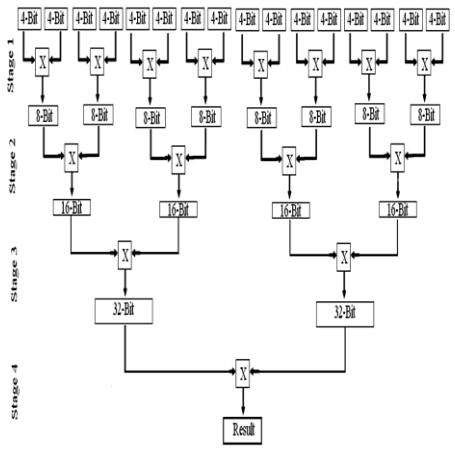

Figure 1: Saha et al Factorial Design

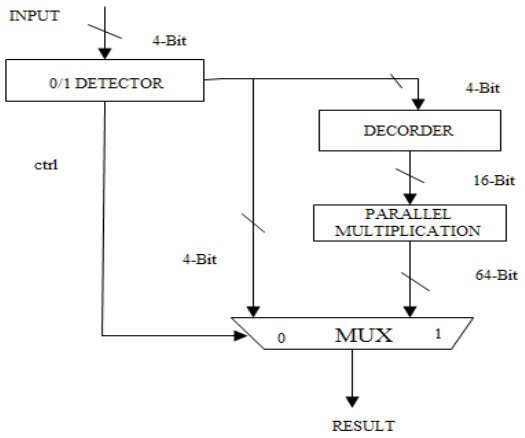

Figure 2: Flow Chart Representation of Low Power Reduced Switching Factorial Circuit

2.1. 0/1 Detector

The schematic representation of 0/1 detector is shown in Figure 3 for the case of a 4 bit input. Here $x(x_3x_2x_1x_0)$ denote the input bits and Ctrl & $y(y_3y_2y_1y_0)$ represent the output bits. The logic that define the outputs of 0/1 detector are given as in Equation (1) to Equation (5).

$$Ctrl = x_3 + x_2 + x_1 \quad (1)$$
$$y_3 = \text{buffered } x_3 \quad (2)$$
$$y_2 = \text{buffered } x_2 \quad (3)$$
$$y_1 = \text{buffered } x_1 \quad (4)$$
$$y_0 = \quad (5)$$

$\overline{Ctrl} + x_0$ The Ctrl output of 0/1 detector is 1 for input greater than one. In case of zero/one input, the output bit y_0 is set to 1. The 0/1 detector output is sent to multiplexer and decoder. Ctrl output is used as the select signal for the output multiplexer. In case of input equal to zero/one, Ctrl will be "0" and the 0/1 detector output is bypassed from the multiplier and sent out directly. For inputs greater than 1, Ctrl will be "1" and the 0/1 detector output will be processed by decoder and parallel multiplier circuitry for factorial computation and the result is passed through multiplexer.

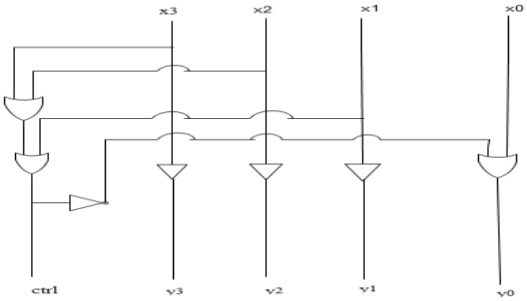

Figure 3: Schematic of 0/1 detector

2.2. Decoder

The decoder circuitry used in the proposed design decides the operation of parallel multiplier. The decoder circuit produces 2^k bit output for a k bit input. For $i < k$, the first 2^i bits are set to 1 and the remaining $2^k - 2^i$ bits are set to zero. For an example let k=4, i=3, here the first 8 output pins of 16 bit decoder will be set to one. The output of the decoder is used as the control input for tri-state buffer used in the proposed parallel multiplier circuit. The tristate buffer passes the input to the multiplier based on the output of decoder . Thus a one at the decoder output enables corresponding multiplier whereas a zero at the decoder output disable the multiplier. The logics that defines the decoder outputs for a 4 bit design are shown in Equation (6) to Equation (18).

$$S1 = y0+y1+y2y3 \quad (6)$$
$$S2 = y0+y1 \quad (7)$$
$$S3 = y0+y1(y2 + y3) \quad (8)$$
$$S4 = y0+y1y2 \quad (9)$$
$$S5 = y0+y1y2y3 \quad (10)$$
$$S6 = y0 \quad (11)$$
$$S7 = y0(y1+y2 + y3') \quad (12)$$
$$S8 = y0(y1+y2) \quad (13)$$
$$S9 = y0(y1+y2y3) \quad (14)$$
$$S10 = y0y1 \quad (15)$$
$$S11 = y3y2(y1 + y0) \quad (16)$$
$$S12 = y3y2y1 \quad (17)$$
$$S13 = y3\ y2y1\ y0 \quad (18)$$

3. proposed parallel multiplier

The advantage of parallel multiplication for factorial calculation is claimed in Saha et al (2011) design. However Saha et al's design suffers from the drawback that irrespective of the value of input all the multipliers are activated. This results in unwanted switching even for small values of input, dissipating huge dynamic power. To reduce this, in the proposed design tristate buffers and multiplexers are used to activate multiplier circuits only when required and is shown in Figure 4 where i represents the position of the multiplier block.

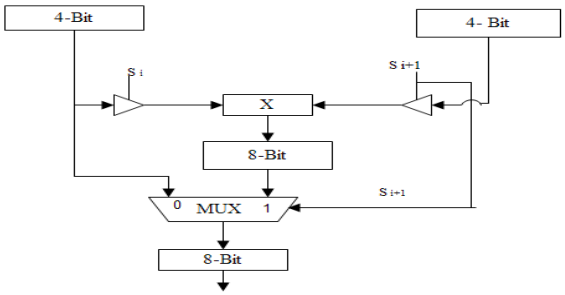

Figure 4: Proposed multiplier design using tri-state buffer

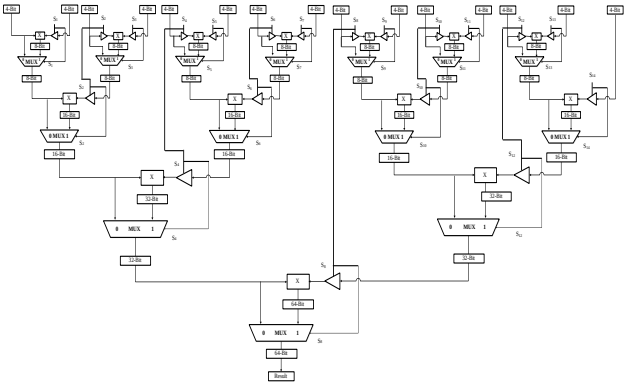

Figure 5: Parallel Multiplier used in proposed Factorial design with $n = 4$.

The constant inputs to the multiplier are stored in 4bit registers . The outputs of registers are passed to the multiplier using tri-state buffers. The decoder outputs are used as the control inputs for tri-state buffer (S_i and S_{i+1}). If both S_i and S_{i+1} are one, inputs are fed to the multiplier circuit.

In case one of the multiplier input has to be zero, the corresponding tri-state buffer control signal S_{i+1} will be set to '0' by decoder and corresponding buffer will be in high impedance state. In this case there will not be switchings in the multiplier and

the bits in the first 4-bit register are passed through the multiplexer to the output register. Figure 5 shows the hardware implementation of parallel multiplier used in 4 bit factorial circuit based on the above approach.

3.1. Optimization of Multiplier

To optimize the performance of the parallel multiplier circuit, 'Vertical and crosswise' sutra [3] of ancient vedic mathematics is used. To claim the advantages of Vertical and crosswise sutra 4 bit multiplication is considered as an example. The partial product generation for the case of 4 X 4 array multiplication is shown in Figure 6. Using carry save addition technique [2] the partial products are added in two stages. The same multiplication realized using "Vertical and Crosswise" sutra results in partial product array as shown in Figure 7.

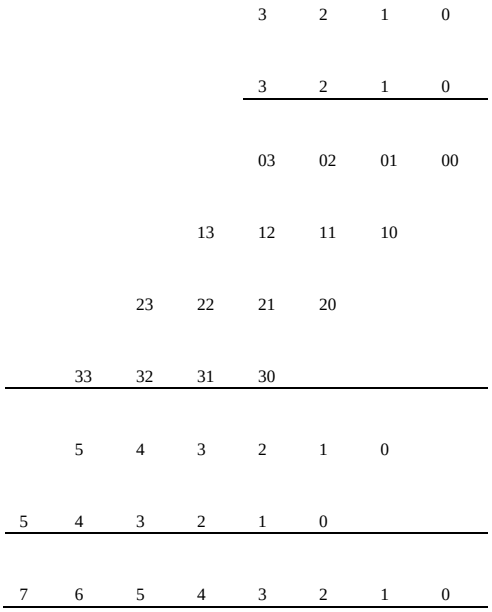

Figure 6: Partial product array for 4 X 4 multiplication

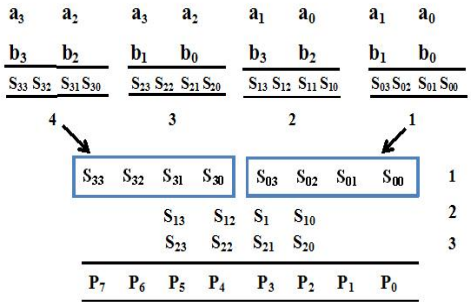

Figure 7: Partial product array for 4 X 4 multiplication using vertical and crosswise sutra

An evaluation of number of AND gates and Full adders used in conventional design and multiplier using "vertical and crosswise " sutra[3] of vedic mathematics for various bitwidths(n = 2,3,4,8) are shown in Table 1. It is seen that the "vertical and crosswise" sutra for multiplication reduces the number of addition operations compared to conventional design, irrespective of the bitwidth of the input. So vedic multiplier[4] is used in the proposed factorial design.

Table 1: Comparison of Conventional array and Vedic multiplier for various bitwidths of input

	Conventional		Vedic	
	No. of AND gates	**No. of Full Adders**	**No. of AND gates**	**No. of Full Adders**
	4	2	4	**1**
	9	7	9	**5**
	16	15	16	**9**
	64	77	64	**53**

4. Experimental results

The VHDL description of the proposed factorial design is done using structural VHDL code and synthesized using Altera Quartus II. Saha et al(2011) factorial design is used for comparison. The performance metrics of the proposed factorial design and design used for comparison are estimated in terms of area, power dissipation and worst case delay, and are shown in Table 2. It is seen from Table 2 that the proposed design and its optimized version shows an area reduction of 39.3% and 46.9% respectively compared to Saha et al(2011) design . The delay and power dissipation of the proposed factorial design reduces by 39.3% and 8% compared to Saha et al (2011) design. Also note that Saha et al(2011) using proposed AEFBC demonstrate better performance in terms of power and delay reduction with the PDP reducing by 4.7% compared to basic Saha et al(2011) design. However the optimized version of the proposed factorial design shows a little higher power dissipation compared to its basic version. The reduced delay and switching of the proposed multiplier reduces energy dissipation of proposed and optimized factorial design by 28.9% and 30.7% respectively.

Table 2: Comparison of Power, Delay and Area of Proposed Factorial designs and previous approach

Parameter / **Factorial circuits**	**Area(No. of LE's)**	**Delay(ns)**	**Power(mW)**	**PDP(pJ)**
Saha et al design(2011)	2292	69.064	133.13	9194.5
Saha et al design(2011)[using AEFBC]	2193	66.2	132.4	8764.9
Proposed design	1391	53.905	121.25	6535.4
Optimized version(Using vedic algorithm)	1218	51.6	123.5	6372.6

5. Implementation of proposed factorial calculator in permutation and combination circuit

To verify the functionality of the proposed area efficient low power factorial circuit an implementation in Permutation and Combination calculator is done and is shown in Figure 8. The factorial block of the Permutation and Combination circuit is implemented with the proposed low power reduced switching factorial calculator. To evaluate the performance of the proposed factorial calculator implemented Permutation and Combination system, Saha et al(2011) factorial calculator is used.

The performance estimates of the proposed factorial implemented Combination and Permutation block and Saha et al's factorial design implemented Combination and Permutation design in terms of power dissipation, area and delay are shown in Table 3. Note that from Table 3, the combination and permutation system implemented with

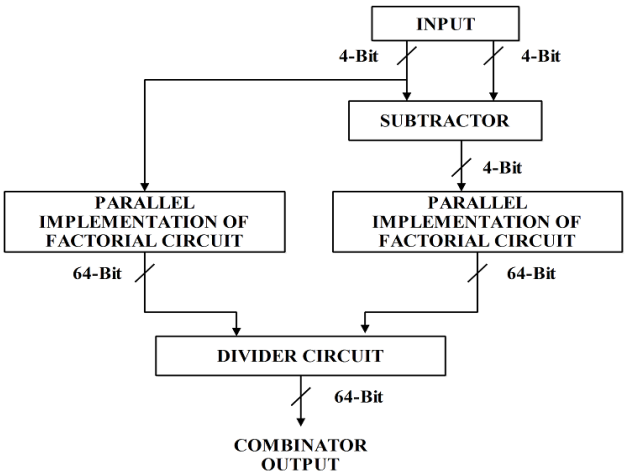

Figure 8: Block diagram of Combination and Permutation calculator

Table 3: Comparison of Power, Delay and Area of proposed and Saha et al Factorial design implemented Combination and Permutation Circuit

Parameters / Combination & Permutation circuit	Area(No. of LE's)	Delay(ns)	Power(mW)	PDP(pJ)
Using Saha et al's Factorial design	7142	924.457	163.35	151010.5
Using Proposed Factorial circuit	6002	903.13	154.44	139479.4
Using Optimized Factorial design	5976	874.53	157.32	137581.1

basic and optimized versions of proposed factorial design exhibit significant area and PDP reductions by atleast 16% and 7.6% respectively compared to Saha et al's design implemented system. This in turn suggests the suitability of proposed factorial designs for low power and high speed applications.

6. Conclusion

A low power and area efficient architecture for factorial computation based on reduced switching parallel multiplication approach is proposed in this chapter. The optimized version of the proposed design combines the advantages of ancient Vedic mathematics for multiplication to further optimize the performance parameters. This inturn combined with parallel implementation methodology lead to significant reduction in the number of stages, resulting in high speed operation and lesser hardware complexity. The average power dissipation of the proposed factorial circuit is found to be 123.5 mW with the corresponding delay of 51.6 ns for 4 bit implementation. This inturn reveals a PDP reduction of the proposed factorial circuitry to be 30.7%. . This suggests the suitability of the proposed factorial design for portable applications. An implementation of the proposed factorial design in Combination and Permutation is done to evaluate its functionality.

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