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Research paper

CTS-SRAM: Design of Low Power CMOS Transmission Gate and Sleep Transistor based SRAM Cell

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Abstract

In modern technology era, the demand for Static Random Access Memory (SRAM) cells has been greatly increased due to its wide variety of applications. Power consumption, speed, read stability and leakage issues are the major design challenges related to SRAM. This paper presents a novel SRAM cell based on Multiple Supply Voltages and non-precharged RBL (MS-N10T) and also shows the comparison of various SRAM cells based on lector, sleep transistors and Transmission gate (TG) to reduce the power consumption when compared to LP10T. The SRAM cell MS-N10T when used in combination of TG and sleep transistors (TGNS-13T) further reduces the power consumption. The analysis further shows that the SRAM, TGNS13T reduces the power consumption approximately by 70-80%. On the Other hand, the LC14T SRAM cell enhances the stability approximately by 80-85%. The major objective of this work is to reduce the power consumption with marginal increase in propagation delay and to improve read stability so as to meet the challenges of advancements in technologies. All the various SRAM architectures are implemented using Cadence 45nm CMOS technology.

Keywords: *CTG-12T; LP10T; LC14T; MS-N10T; Precharge; TGS-14T and TGNS-13T.*

1. Introduction

Presently, there is a great demand for the portable devices such as mobiles, laptops and notebooks etc. which usually operate on high speed batteries. The major reason for this growth in the usage of these devices is due to the data processing that includes text, images, audio and video etc. To overcome the challenges of battery operated systems such as their restricted size, short battery life time and notable power consumption, low power techniques are essential [1]. Among these challenges, the power dissipation is one of the most important bottlenecks with respect to performance, reliability, packaging, cost and portability of the systems.

The explosive demand for battery operated systems shows the increase in the usage of semiconductor memories which are considered to be the basic building blocks of VLSI systems and also acts as a standalone memory. This huge demand of memory is because of its flexibility in storage of the data.

Semiconductor memory is a digital device that is able to store and retrieve the data. Static Random Access Memory (SRAM) plays a key role in order to achieve high performance and low power VLSI applications. It has the capability to provide high performance by maintaining the low standby power consumption and is used when we require fast speed without refreshment repeatedly. A high speed SRAM cell suffers from the dynamic power dissipation and leakage currents. As a result, there will be reduction in battery backup life of the portable devices due to this undesirable power dissipation. Hence, SRAM cell design should have both low static and dynamic power dissipations.

The static power dissipation occurs when the circuit is unused/ inoperative. It consists of leakage currents that occur due to the reverse biased PN junction diode, sub-threshold leakage and tunneling current through gate oxide. Usually, CMOS technology has been honoured for its low static power.

On the other hand, the dynamic power dissipation occurs when the circuit is operative i.e., when particular task has to be performed on providing the input data. It is further divided into signal transitions and short circuit currents which flow from the supply to ground.

One of the most popular methods to reduce the power dissipation is to limit the operating voltage. In addition to reducing the supply voltage, the switching activity and the device size must also be reduced. Besides, the scaling of the supply voltage maintains the power consumption within the range. However, the high performance requirement limits the supply voltage.

The more challenging in the scaled technologies is to maintain the high SRAM yield and stability of the cell as they are specifically attacked by process variations. By using the (i) small sized transistors and (ii) lowering the supply voltage (V_{DD}), the SRAM area and power consumption are reduced. These both methods decrease the noise margin and increase the tolerant capacity to process variation but area is increased because designing a cell for improved stability needs a larger cell area.

The rest of the paper is organized as follows: Section 2 describes the conventional SRAM cell designs and LP10T. Section 3 presents the various novel SRAM cell designs. Section 4 shows the simulation results and comparison. Finally, a brief conclusion is presented in Section 5.

2. Conventional SRAM cell designs and low power 10T (LP10T) SRAM

This section describes the various SRAM cell topologies such as 6T, 8T, 9T, MTCMOS- 9T, 10T, 10T-S and LP10T.

2.1. 6T SRAM

The conventional six transistor (6T) SRAM [1] is as shown in the Fig.1. It doesn't require refreshment repeatedly, hence the name static whereas, dynamic RAM has to be refreshed periodically.
It is formed by the two cross coupled inverters (INV1&INV2) and the two access transistors (M1&M2). The positive feedback of cross-coupled inverters behaves as a fundamental memory device such as latch (or) flip-flop that can store 1 bit information 1 (or) 0. These inverters are comprised of two pull-up transistors (M3&M5) and two pull-down transistors (M4&M6). The cross coupled inverters are connected to the complementary bit lines (BL&BLB) through the access transistors. BL and BLB are specified as the data lines. The gate terminals of the access transistors are connected to the wordline (WL) to either write the data into memory cell (or) read from the cell. The internal nodes (Q&QB) within the circuit, ever maintains the complementary values. Depending on the WL value, the access transistors are turned ON (or) OFF.

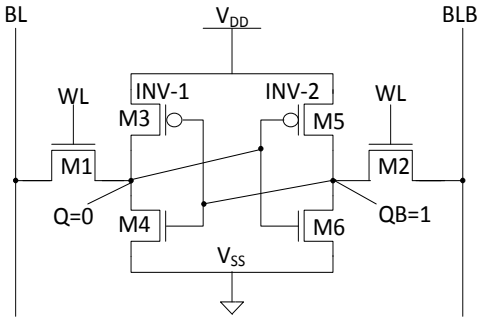

Fig. 1: 6T SRAM

Limitations
Issues related to read and write have been observed. Moreover, since the read current transits over the cell intrinsic node, there exists inherit RSNM problem and also independent transistor sizing is not possible.
Fig.2 shows the read port of 6T SRAM that focuses on the internal node Q in the read current path. To enhance the SRAM bit cell stability and to bring down the leakage currents and power consumption compared to 6T SRAM, various SRAM bit cells and techniques have been proposed.

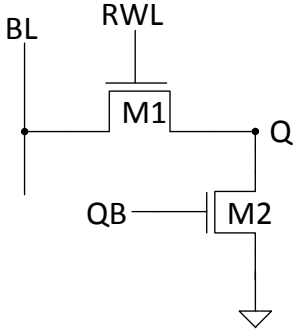

Fig. 2: 6T SRAM read port

2.2. 8T SRAM

It is extension to the 6T SRAM as shown in the Fig.3 and is formed by adding two N-MOS transistors (M1&M2) to the basic 6T SRAM cell [2]. The 8T SRAM cell consists of two separate read and write word lines. Therefore, it can perform the dual-port operation along with read and write bit lines. The internal nodes are not disturbed during the read mode, so that the worst case stability condition is eliminated. Write mechanism to the cell is carried out by the write access transistors and the write bit lines. These write access transistors are controlled by the write wordline. Read mechanism to the cell is carried out by the read access transistor and is controlled by read wordline, RWL. The RBL is precharged prior to the read operation.

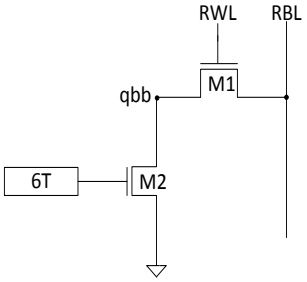

Fig. 3: 8T SRAM read port

The basic stability issue encountered during the read mode of 6T SRAM overcomes in the 8T SRAM. It provides a substantial development in stability during the read operation, without compensation in performance as this operation is carried out by a separate read port. Hence, high RSNM is retained. Besides, the write margin of both these cells is similar because of unaltered write configuration. As, it is composed of separate read and write ports, the transistor sizing of read port can be performed independently without influencing the write performance. Additionally, it yields strong benefits at low supply voltage V_{DD}.
Due to the demand of higher potential difference, 8T SRAM cell exhibits the similar dynamic power dissipation as that of 6T SRAM cell. The read port of 8T is sized broader in order to provide the higher I_{read}, to develop the differential voltage in the similar time (T_{read}) and to produce the equivalent operation. A drawback of area is experienced, due to the two additional transistors.

2.3. Single Ended 9T SRAM

A dedicated 3T read port is appended to conventional 6T SRAM cell [4], to form 9T SRAM as shown in the Fig.4. It uses a strategy with separate read and write word lines. An N-MOS transistor (M2) is added between the transistors (M1&M3) due to which, the read SNM is retained without affecting the write operation. This configuration decreases RBL leakage significantly by the so-called stack effect when (M1 & M2) are OFF. It acquires dynamic power dissipation and write performance same as that of 8T. But, delay is increased when compared with 6T and 8T because of 3T read port.

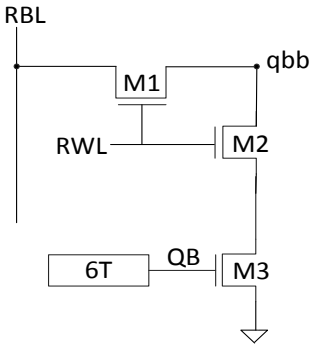

Fig. 4: 9T SRAM read port

2.4. MTCMOS -9T SRAM

Further, a 9T Multi-Threshold Complementary Semiconductor (MTCMOS) SRAM is depicted in the Fig.5 [3]. It is composed of a 6T SRAM cell and an isolated read port .The read port can be obtained with the help of three N-MOS transistors (M1, M2

&M3).Write operation of this cell is similar to the 6T SRAM cell. While read operation, is enabled by activating the read wordline and is followed by conditional RBL discharging. When Q carries logic '0', M3 is turned ON and RBL is discharged to ground. On contradictory, if Q holds logic '1', M2 is enabled and pull up current is provided from RWL (=V_{DD}) to RBL, which slows down the discharging speed of RBL.

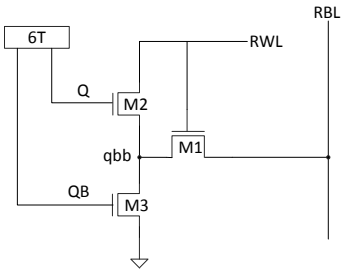

Fig. 5: MTCMOS-9T SRAM read port

It decreases the bit line leakage and improves the bit line sensing margin. Yet, it has the dynamic power same as the 6T SRAM and the total static power is raised.

2.5. 10T SRAM

A 10T SRAM cell is a combination of 6T and 4T [5] as shown in the Fig.6. The transistors (M1 through M4) act as a buffer which is used to read.

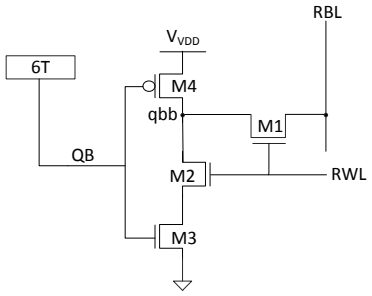

Fig. 6: 10T SRAM read port

The main advantage of this 10T SRAM is that, it provides ultralow leakage for sub threshold operation and effectively reduces the RBL leakage, at the expense of area and performance.

2.6. 10T Single Ended SRAM (10T- S SRAM)

The use of single ended 10T SRAM reduces the readout power and increases the operating frequency when compared to 8T SRAM. Fig.7 shows the 10T non-precharge SRAM with a single ended RBL [6]. A dedicated inverter and transmission gate appended to the conventional 6T SRAM, make up the 10T-S SRAM. The transmission gate is operated with the help of two control signals (RWL&RWLB). The transmission gate is switched ON, when both the control signals are enabled and this results in the connection of stored node of a 6T SRAM to RBL through an inverter.

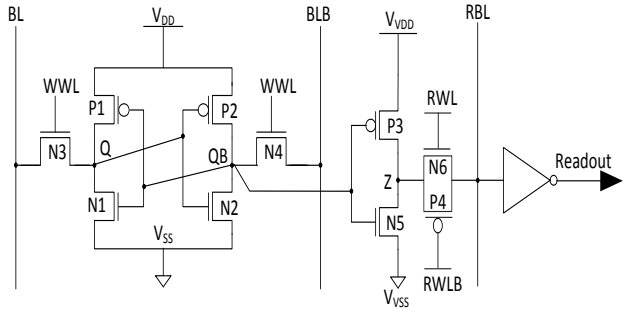

Fig. 7: Schematic representation of 10T-S SRAM

The bit line power is degraded when consecutive 0's and 1's are read out. Only when the readout data is changed, the charge (or) discharge power consumption occurs. An inverter is used to fully charge (or) discharge. As a result, no precharge circuit is required. However, the operating speed is less when compared to 10-T differential and 8T SRAM cell.

2.6. Low Power 10T SRAM (LP10T SRAM)

This bit cell is modified version of above shown 10T-S SRAM [7] which is depicted in the Fig.8 where, RBL is precharged to half V_{DD}. As a result, only a small voltage difference is yielded for every read cycle. The theme of this design is to "charge (or) discharge the RBL from V_{DD}/2 for every read operation". The design is composed of a 4T read port (INV and TG) that is appended to 6T SRAM cell to dissociate the internal nodes Q and QB during the read operation. The internal node of 6T SRAM i.e., QB handles the inverter (P1-N1).The read control signals (R&RB) controls the transmission gate (TG). During the read operation, the output of the inverter (Z) is fixed to RBL through TG. Moreover, 4T read port is powered by dynamically controlled virtual power rails, V_{VDD} and V_{VSS}. Both the virtual rails have the similar precharge levels of RBL to reduce the RBL leakage.

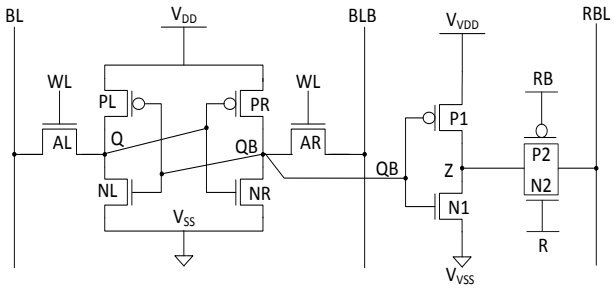

Fig. 8: Schematic representation of LP10T SRAM

Working Operation

The boosted read signals (R&RB) are used for the efficient read operation. Hence, the high current flows in both the directions.

Read-1 Operation

If R and RB reaches high and low respectively then, TG is switched ON to connect RBL to node Z. When QB is '0', then N1 is switched OFF and P1 is switched ON to connect node Z to V_{VDD}, which is high for the read operation. Therefore, through P1 and TG, the read current proceeds from V_{VDD} (=V_{DD}) to RBL (=V_{DD}/2). Hence, RBL voltage rises towards the V_{DD} level. Thus, the read-1 operation is obtained.

Read-0 Operation

For read-0 operation, if QB=1 then, P1 is turned OFF and N1 is turned ON to connect node Z to the V_{VSS}, which is low during the read operation. Hence, the read current flows through TG and N1 from RBL (=V_{DD}/2) to GND. Therefore, the RBL voltage degrades towards 0V.

Due to the half-V_{DD} swing available for each read operation, the boosted signals are used so as to improve the performance degradation. The output of LP10T is sensed through a sense amplifier along with the reference voltage. The sense amplifier that is referenced at the V_{DD}/2 level differentiates the rise and fall of the RBL. As the TG is used in LP10T, it improves the capability of read-1 operation, because the single NMOS cannot charge well the RBL through P1.

In LP10T, the RBL leakage and the average dynamic read power dissipation is decreased when compared to 6T SRAM. It offers better write performance and stability. LP10T is slightly better when compared to 6T in terms of total leakage current. But, the overall leakage power of the LP10T SRAM is similar to the 6T SRAM.

Limitations
Due to control signals complication, the circuit experiences area and power overheads. In LP10T, read-0 and read-1 delay occurs in inverse manner for the different process corners. In reality, the read delay of LP10T is restricted by read-1 delay, as P1 and TG cannot charge the RBL as efficiently as N1 and TG does to discharge it. Sizing of read port is crucial in terms of the area and performance.

3. Proposed SRAM Bit Cell Designs

3.1. MS-N10T SRAM

The schematic representation of Multiple Supply Voltage – Non Precharge 10T (hereafter referred to as MS-N10T) SRAM bit cell is as shown in the Fig.9. It is constructed using the multiple supply voltages (0.8mV and 0.4mV) and also RBL is not precharged to half-V_{DD} [6]. The functioning of MS-N10T SRAM is similar to the conventional LP10T. The power consumption and the leakage power are gradually reduced when compared to LP10T.

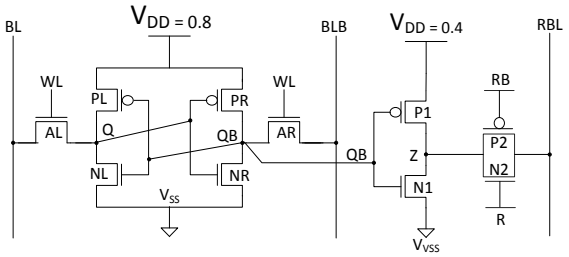

Fig. 9: Schematic representation of MS-N10T SRAM

To further reduce power consumption, the various SRAM cells are implemented based on MS-N10T SRAM.

3.2. LC-14T SRAM

The schematic representation of Leakage Control 14T (hereafter referred to as LC14T) SRAM bit cell which employs Lector technique [8] is as shown in the Fig.10. The lector technique works on the principle that "A circuit in which more than one transistor is OFF between power supply and ground path shows the less leakage power when compared to the circuit in which only one transistor is OFF between power supply and ground". The configuration of this SRAM is alike MS-N10T, but the only distinction is that LC-14T SRAM consists of a pair of CMOS inverters based on leakage control transistors (LCTs). This SRAM consists of LCTs - P2, N1, P4 and N3 connected in between the transistors P1, N2, P3 and N4 respectively. The gate terminal of each LCT is connected to the source terminal of another LCT. When BL=0, BLB=1 and WL=1, then P2, N2, P3 and N3 are turned ON while P1, N1, P4 and N4 are turned OFF. When BL=1, BLB=0 and WL=1, then P1, N1, P4 and N4 are turned ON while P2, N2, P3 and N3 are turned OFF.

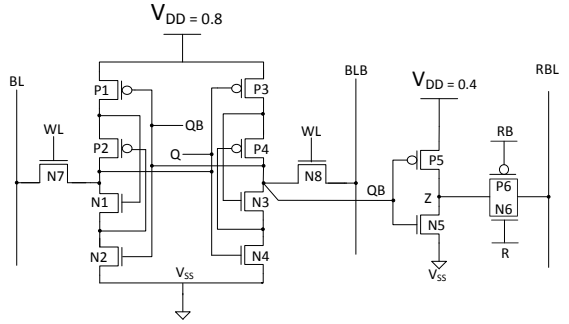

Fig. 10: Schematic representation of LC-14T SRAM

The power consumption and the leakage power of LC14T are reduced while the stability is greatly increased when compared to LP10T. In order to still reduce the power consumption we are opting for CTG-12T SRAM.

3.3. CTG-12T SRAM

CMOS Transmission Gate 12T (hereafter referred to as CTG-12T) SRAM [9] is as shown in the Fig.11. The operation of CTG-12T SRAM resembles MS-N10T SRAM but only difference is that the access transistors of SRAM are replaced by the CTGs - P5, N5, P6, and N6. Hence, the CTGs are controlled by two control signals (WL&WLB). These signals are complement to each other.

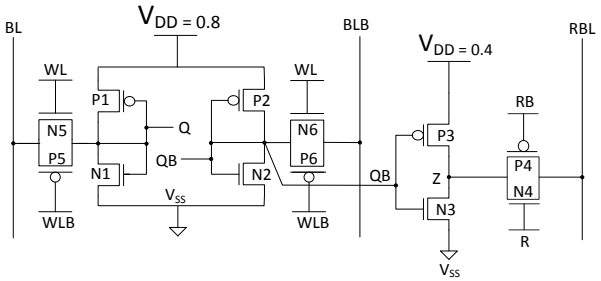

Fig. 11: Schematic representation of CTG-12T SRAM

This design shows the reduced power consumption, leakage power and increased stability when compared to LP10T.

3.4. TGS-14T SRAM

To increase the stability compared to CTG-12T SRAM, TGS-14T (TG + Sleep transistors) SRAM [10] is considered. This circuit is based on MS-N10T SRAM with the combination of Transmission Gate (TG) and sleep transistors which is as shown in the Fig.12. A P7 is connected at the top and N7 is connected at the bottom of the cross coupled inverters. These sleep transistors can be operated with the help of (V_{SP}&V_{SN}) signals. In sleep mode i.e., when the sleep transistors are turned OFF, there exists no connection between the power supply V_{DD} and ground.

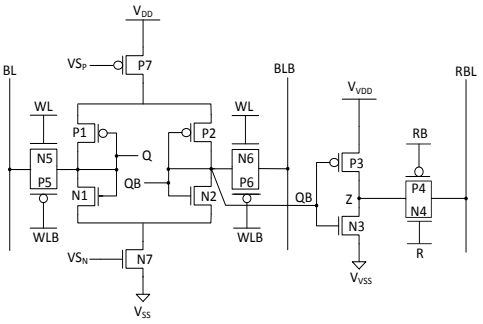

Fig. 12: Schematic representation of TGS-14T SRAM

This design reduces the power consumption and leakage power when compared to LP10T SRAM with increase in the stability. If we detach the sleep transistor P7 between the power supply (V_{DD}) and the SRAM cell while preserving the remaining circuit, the following configuration of TGNS-13T SRAM is obtained.

3.5. TGNS-13T SRAM

Fig.13 shows TGNS-13T (TG + NMOS Sleep Transistor) SRAM [10].The operation of this SRAM resembles the MS-N10T SRAM. The power consumption and leakage power are drastically reduced whereas the stability is increased compared to LP10T SRAM.

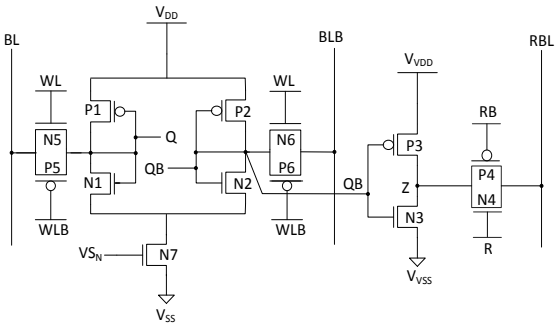

Fig. 13: Schematic representation of TGNS-13T SRAM

4. Simulation Results

Fig.14 shows the transient waveforms of a conventional LP10T. When WL=0, there is no operation performed in the circuit. In contrast when WL=1, either read or write operation can be performed. The RBL is charged or discharged, only when the TG is switched ON. If R is low and RB is high then, TG is switched OFF and the circuit will be in non- read mode.

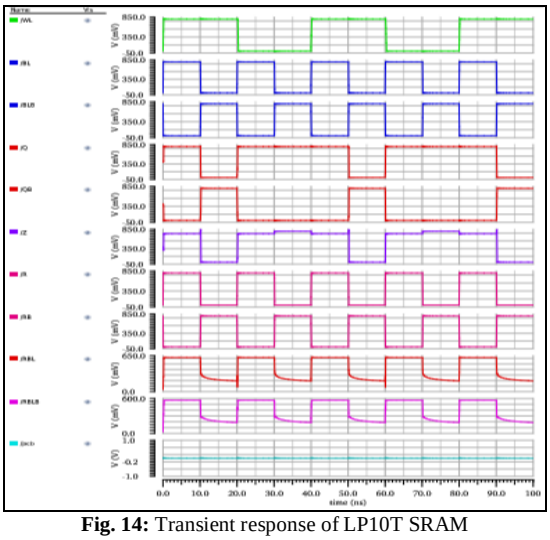

Fig. 14: Transient response of LP10T SRAM

Fig.15 shows the transient waveform of a TGNS-13T (TG + NMOS Sleep Transistor). This configuration is formed by using an NMOS sleep transistor.

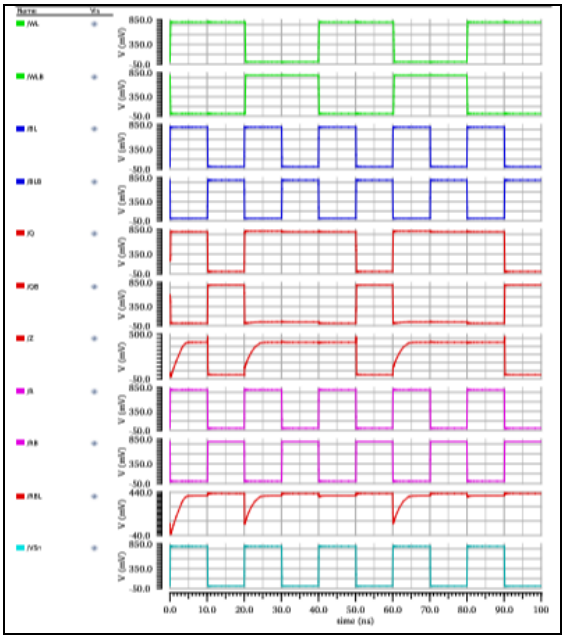

Fig. 15: Transient response of TGNS-13T SRAM

Fig.16 shows the comparison of power consumption in the various novel SRAM topologies. It is observed that the power consumption is gradually reduced using TGNS-13T SRAM when compared to all other SRAM bit cells.

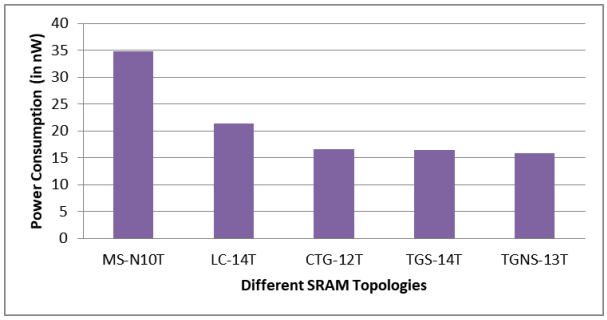

Fig. 16: Power consumption of different SRAMs

Fig.17 shows the read stability of the various proposed SRAM topologies. It is can be seen that the read stability is drastically increased in LC14T SRAM when compared to other SRAM bit cells.

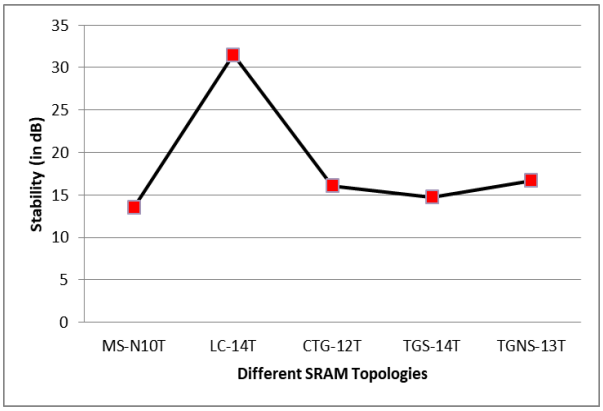

Fig. 17: Stability of various SRAM bit cells

In the Fig.18 power consumption for LC14T, CTG12T, TGS14T, TGNS13T is shown against five process corners (TT,SS,SF,FS,FF) at three different temperatures(°C)-40,27,125. It shows the low power consumption in FF design corner i.e.13.83 (nW) at -40°C.

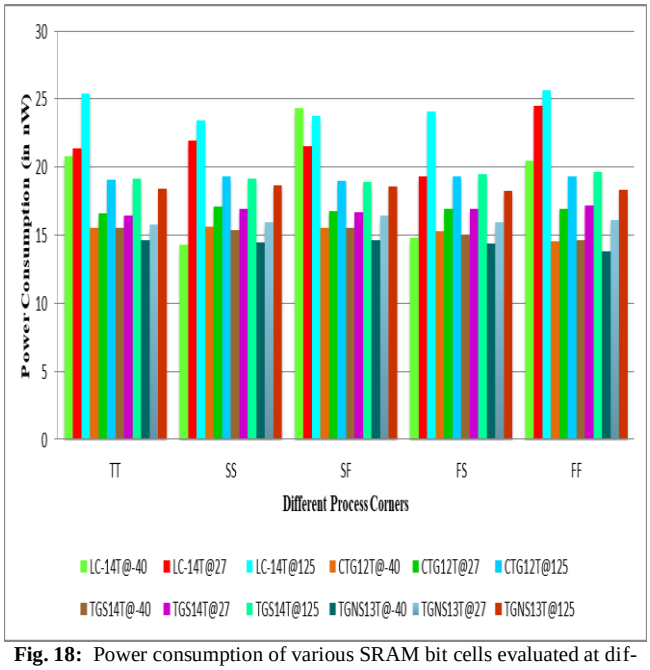

Fig. 18: Power consumption of various SRAM bit cells evaluated at different design corners and temperatures

Fig.19-20 shows the leakage power and leakage current of various SRAM topologies. It is observed that the TGNS-13T SRAM produces the low leakage power and the low leakage current.

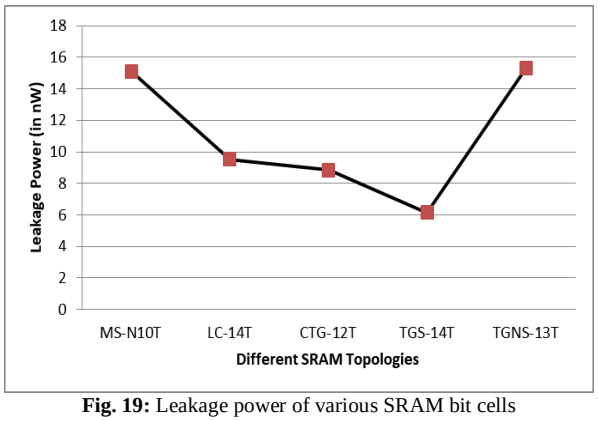

Fig. 19: Leakage power of various SRAM bit cells

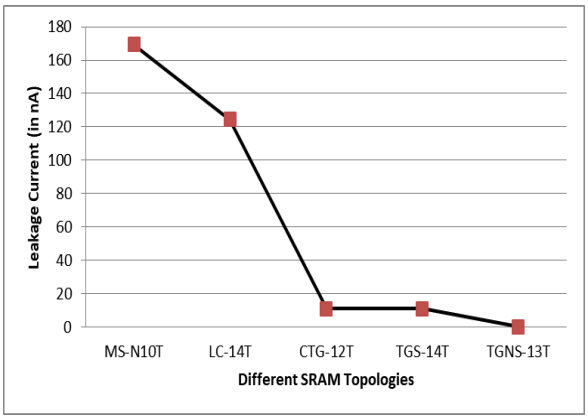

Fig. 20: Leakage current of various SRAM bit cells

Table 1 shows the comparison of total power consumption, stability and leakage power in the various SRAM bit cells. The novel TGNS-13T and LC-14T SRAM provides the reduced power consumption and increased read stability respectively.

Table 1: Power, Stability and Leakage Power of Various SRAM cells

Topology	Total Power (nW)	Stability (dB)	Leakage Power (nW)
LP10T	1029	13.535	22.68
MS-N10T	34.86	13.507	15.1
LC14T	21.35	31.515	9.53
CTG12T	16.56	16.052	8.84
TGS14T	16.47	14.722	6.154
TGNS-13T	15.78	16.711	15.3

Table 2 shows the power consumption of the different SRAM topologies at three different supply voltages (0.8, 0.7 and 0.6). It is observed that the power consumption is rapidly decreased with the decrease in supply voltage.

Table 2: Power (nW) of Various SRAM bit cells at Different Supply Voltages (mV) cells

Supply Voltage	0.8	0.7	0.6
LP10T	1029	420.2	121.2
MS-N10T	34.86	19.95	11.49
LC14T	21.35	13.98	10.59
CTG12T	16.56	14.37	12.32
TGS14T	16.47	14.43	12.23
TGNS13T	15.78	13.94	11.89

5. Conclusion

This paper demonstrates the comparison of the various SRAM bit cells with respect to the power consumption. A novel SRAM bit cell TGNS-13T, that consumes the less power when compared to the LP-10T SRAM is proposed. This configuration achieves reduction in power approximately by 70-80% i.e., from 1029(nW) to 15.78(nW). Another important parameter affecting the performance of an SRAM is stability (dB), which is enhanced by using the configuration of LC-14T SRAM. As a result, the stability is improved approximately by 80-85% i.e., from 13.535(dB) to 31.515(dB). However, the novel designs incur area as the transistor count is more when compared to the conventional design (LP10T). Therefore, based on the application, the SRAM cell TGNS13T can be considered for reducing the power consumption and LC-14T SRAM can be chosen to improve the stability when compared to the LP10T SRAM.

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