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Research paper

Low-load Efficiency Improvement of a Three-Phase Bidirectional Isolated DC-DC Converter (3P-BIDC) Via Enhanced Switching Strategy

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Abstract

This paper presents the system design, operation and enhanced switching strategy of a three-phase bidirectional isolated dc-dc converter (3P-BIDC). The paper discusses the operating modes of the 3P-BIDC using phase-shift modulation (PSM), with analysis on its soft-switching characteristics. The phase-shift modulation is the simplest modulation technique that can be applied to the 3P-BIDC. However, it comes with the consequences of low efficiency performance in the low-load conditions. Therefore, this paper investigates the improvement in efficiency of the 3P-BIDC during low-load condition using an enhanced switching strategy combining burst-mode switching and phase-shift modulation. The model of a 700-V, 100-kW, 20-kHz 3P-BIDC and the enhanced switching strategy are verified via simulation using PSCAD. The simulation results shows that the combination of burst-mode and phase-shift modulation technique improves the efficiency of the 3P-BIDC at low-load conditions.

Keywords: bidirectional isolated dc-dc converter; burst-mode switching; phase-shift modulation; ZVS; switching losses

1. Introduction

A bidirectional isolated dc-dc converter (BIDC) also known as the dual active bridge converter consists of two single-phase (1P) or three-phase (3P) full-bridge voltage-source converters that are galvanically isolated by a single- or three-phase high-frequency transformer. The BIDC plays a significant role in battery energy-storage systems for electric vehicles [1], grid-connected energy storage system [2], and more recently, solid-state transformers [3].

Publications have focused on the improvement in efficiency of 1P-BIDC [4]-[5]. A new topology called the double stacked active bridge (DSAB) is proposed in [6] in order to extend the zero-voltage switching (ZVS) operating range. However, if applied to a three-phase topology, the system may have a more complex design and expensive cost due to the increased number of components.

Figure 1 shows the block diagram of the 3P-BIDC. The two DC-link capacitors can handle high switching current ripples and maintain a nearly constant DC bus voltage. The three-phase bidirectional isolated dc-dc converter (3P-BIDC) has been less popular as compared to the single-phase topology because of a challenge in the practical realization of the three-phase high-frequency transformer with uniform leakage inductance. However, a 3P-BIDC is more attractive for high power density intensive applications such as in the automotive applications [7], MVDC shipboard power systems [8], LVDC power systems [9] and railway applications [10]. The 3P-BIDC performs better than the single- phase BIDC when operated using the phase-shift modulation because the total input and output

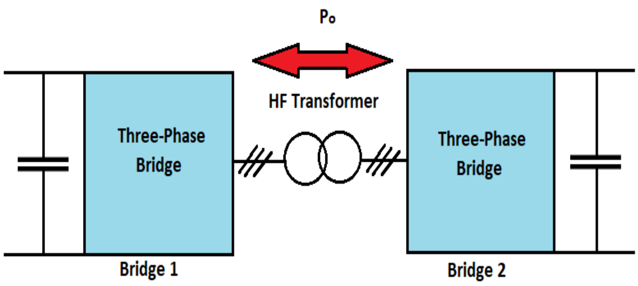


Fig. 1: 3P-BIDC block diagram.

filter requirements are lower [11]. The switching stress is distributed in the 3P-BIDC to about 1/3 of the switching stress in the 1P-BIDC [12].

Phase-shift modulation (PSM) has been traditionally used to operate the 3P-BIDC. The technique is simple to understand and implement. The PSM can be simply controlled by adjusting the phase-shift angle δ, which is the angle difference between the two AC phase voltages of bridges 1 and 2 in the 3P-BIDC. The optimum operation of the 3P-BIDC is when the ratio of the DC voltages is equal to its transformer turns ratio. However, when the ratio of the DC voltages are not equal to the transformer turns ratio, the region of high-efficiency is reduced [13]. Therefore, the overall high-efficiency of the 3P-BIDC cannot be maintained over a wide operating voltage and power range.

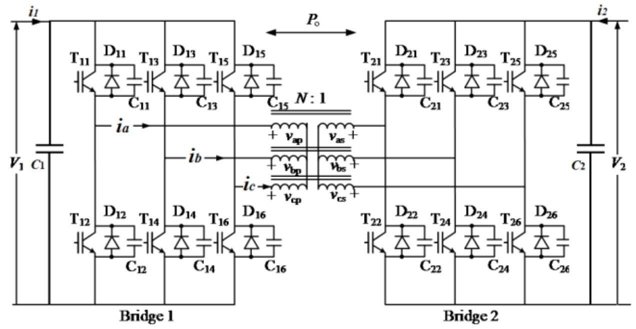


Fig. 2: A three-phase bidirectional isolated dc-dc converter.

Several other switching techniques have been introduced to improve the low-load efficiency of the 3P-BIDC using modulation techniques other than phase-shift modulation. The authors of [14] proposed triangular modulation technique that can increase the area of soft-switching to the low-load operations – from 16.67% of the rated power to the rated power. Moreover, trapezoidal and triangular modulation have been combined with phase-shift modulation to improve the overall efficiency of the converter [1]. However, triangular modulation is feasible only when the ratio of the DC voltages are not equal to the transformer turns ratio. On the other hand, the trapezoidal modulation causes high RMS currents in the BIDC. Both switching strategies are also complex. Therefore, an enhanced switching strategy is required to maintain the overall efficiency of the three-phase BIDC across a wide operating power range.

A burst-mode switching (BMS) strategy has been verified to significantly improve the low-load efficiency of a 1P-BIDC [15]-[16] and also in other types of DC-DC converters [17]-[18]. In BMS, the transistors of the switching DC-DC converter are cyclically switched ON and OFF at a fixed frequency during a conducting period resulting in a burst of energy pulses transferred to the output, but they are permanently in the OFF-state during a non-conducting period [17].

This paper proposes the BMS for a 3P-BIDC. The BMS enables intermittent power transfer to the output during a low-load operation. Two switching strategies namely, the PSM and BMS can work together to provide a wider range of output power for the DC-DC converter to operate efficiently. This paper is arranged such that Sections 2 and 3 explains the 3P BIDC and the basic theory of the phase-shift modulation (PSM) strategy. Section 4 presents the simulation method combining the conventional PSM and the proposed BMS. Section 5 discusses results from the simulation and Section 6 is the conclusion.

2. Three-Phase Bidirectional Isolated DC-DC Converter (3P-BIDC)

Figure 2 shows the basic topology of the 3P-BIDC. It uses six IGBTs on each bridge. Power can be transferred from bridge 1 or bridge 2. The DC-link voltages of bridges 1 and 2 are V_1 and V_2, respectively. The semiconductor switches T_{11}–T_{26} could be an

Table 1: Conducting components in the 3P-BIDC based-on positive-half cycle.

Mode	Bridge 1	Bridge 2
1 ($t_0 \le t < t_1$)	T_{12}, T_{14}, T_{15}	D_{22}, D_{24}, D_{25}
2 ($t_1 \le t < t_2$)	Soft-switching (C_{11} and C_{12})	D_{22}, D_{24}, D_{25}, T_{22}
3 ($t_2 \le t < t_3$)	T_{11}, T_{14}, T_{15}, D_{11}	Soft-switching (C_{21} and C_{22})
4 ($t_3 \le t < t_4$)	T_{11}, T_{14}, T_{15}	D_{21}, D_{24}, D_{25}
5 ($t_4 \le t < t_5$)	Soft-switching (C_{15} and C_{16})	D_{21}, D_{24}, D_{25}, T_{25}
6 ($t_5 \le t < t_6$)	T_{11}, T_{14}, T_{16}, D_{16}	Soft-switching (C_{25} and C_{26})
7 ($t_6 \le t < t_7$)	T_{11}, T_{14}, T_{16}	D_{21}, D_{24}, D_{26}
8 ($t_7 \le t < t_8$)	Soft-switching (C_{13} and C_{14})	D_{21}, D_{24}, D_{26}, T_{24}
9 ($t_8 \le t < t_9$)	T_{11}, T_{13}, T_{16}, D_{13}	Soft-switching (C_{23} and C_{24})
10 ($t_9 \le t < t_{10}$)	T_{11}, T_{13}, T_{16}	D_{21}, D_{23}, D_{26}
11 ($t_{10} \le t < t_{11}$)	Soft-switching (C_{11} and C_{12})	D_{21}, D_{23}, D_{26}, T_{21}
12 ($t_{11} \le t < t_{12}$)	T_{12}, T_{13}, T_{16}, D_{12}	Soft-switching (C_{21} and C_{22})

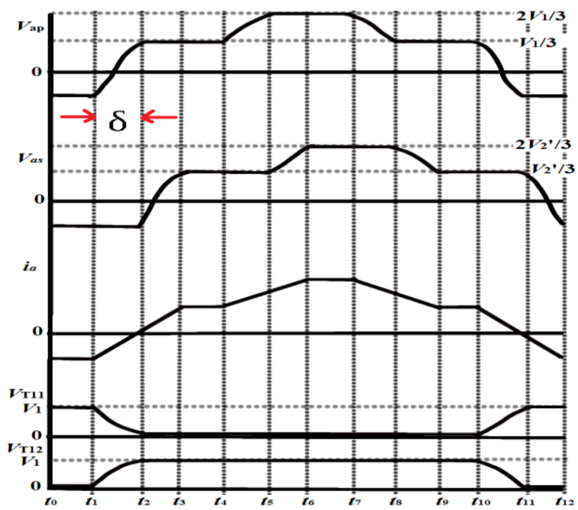
2 are symmetrical and galvanically isolated by a high frequency three-phase transformer of turns ratio N. Compared to the 1P-BIDC, the 3P-BIDC topology may also provide the advantage of power distribution due to the increased number of switches available in the converter. The 3P-BIDC converter has higher power capability and lower ripple current on both input and output side, which leads to lower capacitor volume and higher power density [19]. The average power for the 3P-BIDC when $0° \le \delta \le 30°$ is defined and analysed in [11], [20] and [21]:

$$P_o = \frac{V_1 N V_2}{2\pi f_s L}\delta\left(\frac{2}{3} - \frac{\delta}{2\pi}\right) \quad (1)$$

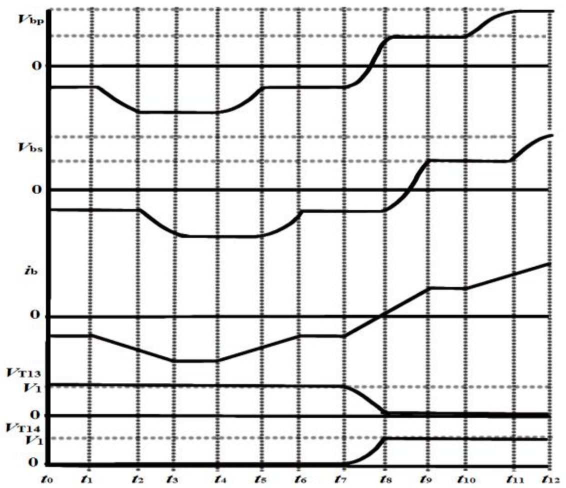
Where δ is the phase-shift angle in radians of the AC phase voltages of bridges 1 and 2, f_s is the switching frequency, and L is the total leakage inductance at each phase referred to bridge 1 side.

3. Operating Principles Based-on Phase-Shift Modulation

In this section, the analysis of the 3P-BIDC operating waveforms are based-on soft-switching through the resonance between the snubber capacitor and transformer leakage inductances in each phase [12]. The authors of [21] assumed the commutations of current in the snubber capacitors to be instantaneous in the operating mode analysis. However, this section includes ZVS in the operating modes. In the 3P-BIDC, dead time is introduced as the duration when both switches in the same leg are in the off state to prevent short circuit to ground.



(a)



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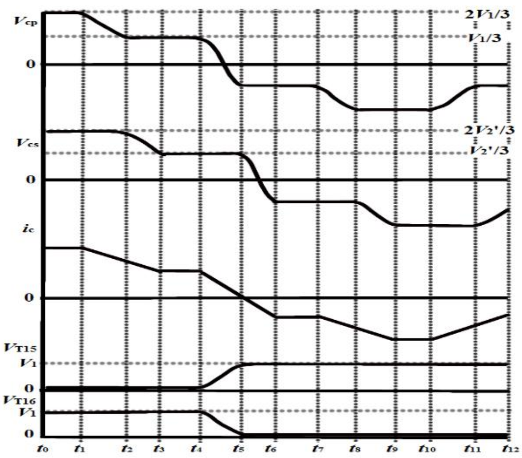


(c)

Fig. 3: Theoretical operating waveforms of the 3P-BIDC. (a) Phase A, (b) Phase B, and (c) Phase C.

The resonance between the snubber capacitors and the transformer leakage inductance takes place within the dead time of the semiconductor switches in the same leg [2], [17]. In this section, the dead time takes place from t_1 to t_2 in phase A, t_7-t_8 in phase B and t_4-t_5 in phase C.

During turn-off, the snubber capacitor is assumed to be large enough to minimize the rate of change of voltage across a semiconductor switch, almost achieving zero-voltage switching (ZVS) at turn-off. During turn-on, ZVS occurs when a gate signal is sent to the semiconductor switch as the converter current is clamped by its anti-parallel diode.

Table 1 shows the operating components of the 3P-BIDC in phase A, phase B and phase C of bridge 1 that correspond to the main operating waveforms shown in Figures 3 (a), (b), and (c) respectively.
The operating modes of the 3P-BIDC consider ZVS operation. The voltages V_{ap} and V_{as} are the AC voltages of phase A in bridges 1 and 2, respectively. Switches T_{11}, T_{12}, T_{21} and T_{22}, their respective body diodes are D_{11}, D_{12}, D_{21}, and D_{22} while the snubber capacitors are C_{11}, C_{12}, C_{21}, and C_{22}. The voltages across the snubber capacitors are
V_{11}, V_{12}, V_{21} *and* V_{22} respectively. The transformer leakage inductances in each phase is denoted by L_a, L_b, and L_c. The time from t_1 to t_2 are the reference points for the phase-shift angle δ.

Mode 1 ($t_0 \le t < t_1$): From t_0 to t_1, the semiconductor switches T_{12}, T_{14} and T_{15} are conducting. V_{ap} is equal to $-V_1/3$. At time t_1, T_{12} is gated-off marking the beginning of the dead time of phase A in mode 2.

Mode 2 ($t_1 \le t < t_2$): The phase current, i_a is negative and flows through T_{12}. Resonance starts to occur between the snubber capacitors C_{11} (C_{12}), and L_a. C_{11} discharges while C_{12} charges. T_{11} is gated on by ZVS.

Mode 3 ($t_2 \le t < t_3$): At t_2, V_{ap} is equal to $V_1/3$. V_{T11} attempts to overshoot to the negative rail and D_{11} is forward biased. After time t_2, Current i_a is positive and supplies energy to V_2.

Mode 4 ($t_3 \le t < t_4$): From t_3 to t_4, the semiconductor switches T_{11}, T_{14}, and T_{15} are conducting. V_{cp} is equal to $V_1/3$. At the end of mode 4, T_{15} is gated to turn-off marking the beginning of the dead time of Phase C in mode 5.

Mode 5 ($t_4 \le t < t_5$): The phase current i_c is positive and supplies energy to V_2. Resonance starts to occur between the snubber capacitors C_{15} (C_{16}) and L_c. C_{15} charges while C_{16} discharges. T_{16} is gated-on by ZVS.

Mode 6 ($t_5 \le t < t_6$): At t_5, V_{cp} is equal to $-V_1/3$. V_{T16} attempts to overshoot to the negative rail and D_{16} is forward-biased. After time t_5, i_c is negative and flows through T_{16}.

Mode 7 ($t_6 \le t < t_7$): From t_6 to t_7, the semiconductor switches T_{11}, T_{14}, and T_{16} are conducting. V_{bp} is equal to $-V_1/3$. At the end of mode
7, T_{14} is gated to turn-off marking the beginning of the dead time of Phase B in mode 8.

Table 2: 3P-BIDC circuit parameters

Parameters	Symbol	Values
Rated Power	P_R	100 kW
Dc Voltage at bridge 1	V_1	700 V
Dc Voltage at bridge 2	V_2	525 V - 700 V
Range of Phase-Shift Angle	δ	$-30 \le \delta \le 30°$
Switching Frequency	f_s	20 kHz
Dc-link Capacitors	C_1, C_2	10 mF
Snubber Capacitors	C_{11}-C_{26}	6 nF
Transformer Turns Ratio	N:1	1:1
Transformer Leakage Inductances (each phase)	L_a, L_b, L_c	11.91 μF (0.20 pu)

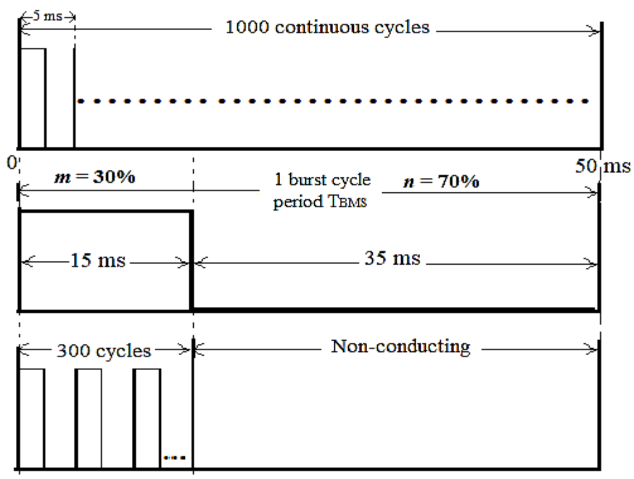


Fig. 4: Generation of BMS signals by multiplying 1000 20-kHz with one 20-Hz burst signal having a conduction period of m = 30%.

Mode 8 ($t_7 \le t < t_8$): The phase current i_b is negative and flows through T_{14}. Resonance starts to occur between the snubber capacitors C_{13} (C_{14}) and L_b. C_{13} discharges while C_{14} charges. From t_7 to t_8, T_{13} is gated-on by ZVS.

Mode 9 ($t_8 \leq t < t_9$): At t_8, V_{bp} is equal to $V_1/3$. V_{T13} attempts to overshoot to the negative rail and D_{13} is forward-biased. After t_8, i_b is positive and flows to L_b via T_{13}.

Mode 10 ($t_9 \leq t < t_{10}$): From t_9 to t_{10}, the semiconductor switches T_{11}, T_{13} and T_{16} are conducting. V_{ap} is equal to $V_1/3$. At the end of mode 10, T_{11} is gated to turn-off marking the beginning of the dead time of phase A in mode 11.

Mode 11 ($t_{10} \leq t < t_{11}$): The phase current i_a is positive and La supplies energy to V_2. Resonance starts to occur between the snubber capacitors C_{11} (C_{12}) and L_a. C_{11} charges while C_{12} discharges. From t_{10} to t_{11}, T_{12} is gated on by ZVS.

Mode 12 ($t_{11} \leq t < t_{12}$): At t_{11}, V_{ap} is equal to $-V_1/3$. V_{T12} attempts to overshoot to the negative rail and D_{12} is forward-biased. After time t_{11}, i_a is negative and flows through T_{12}.

Note that in a practical system, hard-switching and incomplete ZVS is likely to occur. Hard-switching operation may occur in the DC-DC converter during light-load conditions whereas incomplete ZVS occurs when the snubber capacitors of one leg in a bridge does not completely discharge to zero voltage, when a semiconductor switch is turned on.

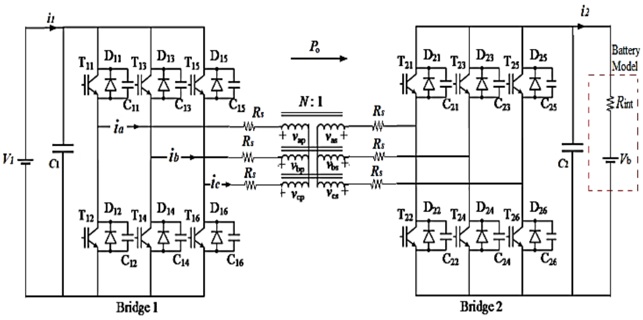


Fig. 5: The simulation model

4. Simulation Model and Proposed Enhanced Switching Strategy

The proposed strategy combines two switching techniques. In the medium to high power transfer region, 20% of rated power to the rated power, only phase-shift modulation is employed. In the low power transfer region, less than 20% of the rated power, the combination of BMS and PSM is employed. The simulation model verification is carried out using PSCAD software. Moreover, efficiency measurement is also carried out in the simulation.

The converter efficiency is calculated as the ratio of the DC output power in equation (3) to the DC input power in equation (2) when power is transferred from bridge 1 to bridge 2.

$$P_{i,DC} = V_1 I_1 \quad (2)$$

$$P_{o,DC} = V_2 I_2 \quad (3)$$

Table 2 presents the circuit parameters of the 3P-BIDC shown in Figure 2. The rated power and voltage of the converter is 100 kW and 700 V respectively. The transformer leakage inductances in each
phase is designed based on equation (1). In this paper, a positive phase-shift angle, δ is assumed when power is transferred from bridge 1 to bridge 2.

Figure 4 describes the theory of generating burst-mode switching (BMS) that enables intermittent power transfer during low-load operation. 300 cycles of burst mode signals with a duty cycle of 30% are generated via the multiplication of two input signals. The BMS is obtained from the generation of 300 cycles of 20-kHz signals with a duty cycle of 50% multiplied with one 20-Hz conduction signal having a period of m = 30%. The BMS in bridge 2 are generated in the same manner. Note that "m" is the conducting period in percentage of the burst mode signal and "n" denotes the non-conducting period in percentage. In the case demonstrated here, "m" is 30% and "n" is 70%. The burst mode switching strategy are simulated and compared with only PSM strategy in low-load conditions. When the conducting period of the BMS is set to 10%, m = 10% and n = 90%. The sum of "m" and "n" should always be 100%.

For low-power operation, BMS is combined with PSM as the enhanced switching strategy. Therefore, the control of the phase-shift angle δ is also required, in addition to the control of m and frequency value of the low-frequency signal.

$$f_{BMS} = 1/T_{BMS} \quad (4)$$

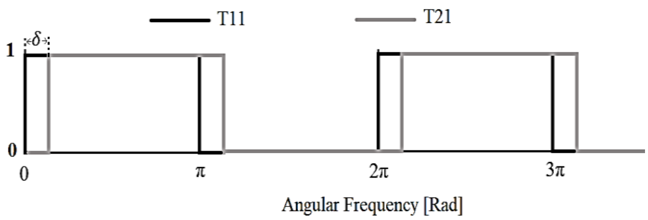


Fig. 6: Gate signals to switches T_{11} and T_{21} at δ=30° using phase-shift modulation.

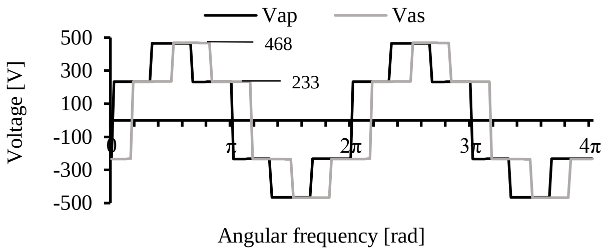


Fig. 7: AC voltages at bridges 1 and 2 using phase-shift modulation at $V_1 = V_2$ = 700 V, δ=30°.

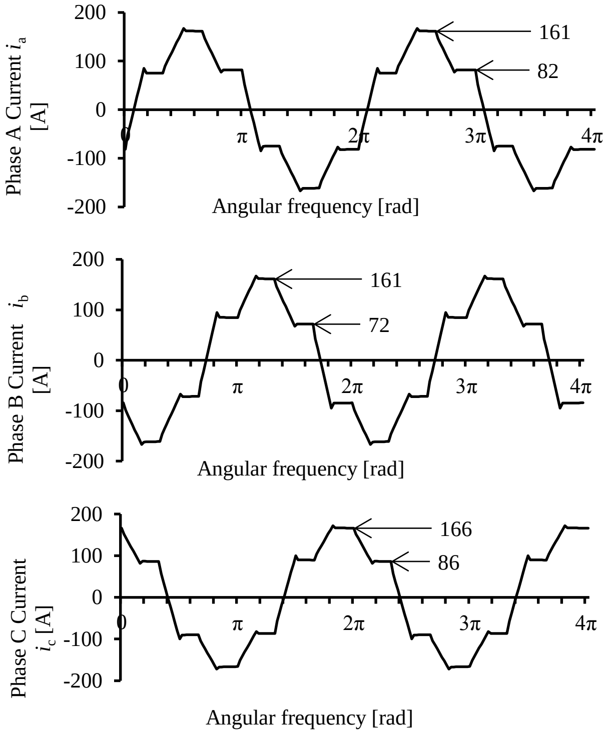


Fig. 8: Inductor current waveforms.

Figure 5 presents the simulation model that is used to verify the proposed enhanced switching strategy. The model is applied for battery charging and discharging. A battery model is connected in the output terminal with a voltage, V_b of 525 V to 700 V and an internal resistance, R_{int} of 5 mΩ. A series resistor, R_s of 100 mΩ is added in series with the transformer leakage inductance. The resistor R_s represents any resistance that may exist in the transformer winding and connection points of a practical converter.

5. 3P-BIDC Simulation Results

This section presents the results obtained from the PSCAD simulation modelling of the 3P-BIDC using PSM and BMS with conducting periods of 10%, 30% and 50%. The simulation for Figures 6 to 9 are at their rated conditions.

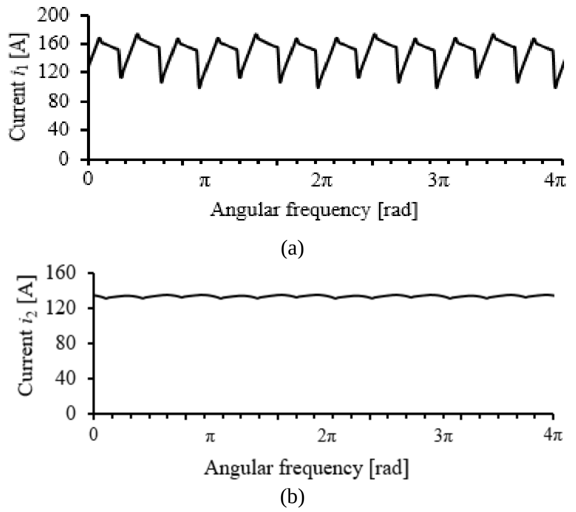


Fig. 9: DC current waveforms using phase-shift modulation. (a) Bridge 1 and (b) Bridge 2.

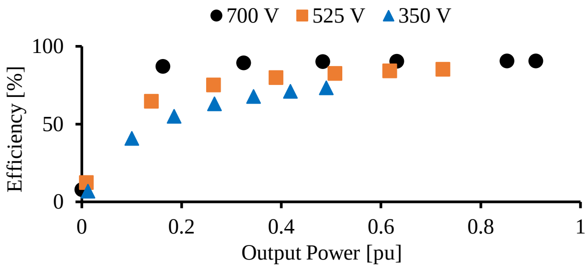


Fig. 10: Efficiency versus output power using PSM for V_b of 700 V, 525 V, 350 V and V_1 = 700 V.

5.1. Phase-Shift Modulation

Figure 6 shows the gate signals for T_{11} and T_{21} using PSM. Both gate signals have duty cycles of 50%. The phase-shift angle δ is varied between -30° to 30°. The feasibility of the PSM using different values of V_2 and δ are investigated. The power transfer from bridge 2 to bridge 1 that is obtained by setting the phase-shift angles from -30° to 0° are verified to transfer the same range of power when the phase-shift angle is $0° \leq \delta \leq 30°$ as the design of the converter is symmetrical.

Figure 7 presents the AC voltage waveform of phase A of bridges 1 and 2. The voltage values of 468 V and 233 V correspond to $2/3V_1$ and $V_1/3$, respectively. The waveforms of bridge 1 leads bridge 2 by 30° phase-shift at the rated power of 100 kW.

Figure 8 shows the high-frequency AC current waveforms in each phase. The current waveforms are phase-shifted by 120° with the peak current at ±160 A at $\delta = 30°$ and $V_b = 700$ V . The AC current waveforms are similar to the theoretical AC current waveforms described in section 2.

Figure 9 presents the input and output DC current waveforms at 30° phase-shift angle. The current i_1 has a ripple of 40% and the current i_2 has a ripple of 2%, when the battery is charged from source V_1 at the rated power. The frequency of the DC current is 40 kHz.

Figure 10 presents the efficiency of the 3P-BIDC using PSM for various battery voltage, V_b of 700 V, 525 V, and 350 V accordingly. Note that the rated output power can only be achieved at $\delta > 30°$ when the magnitudes of V_b is less than 700 V. However, the output current will be increased beyond the converter rated current, which

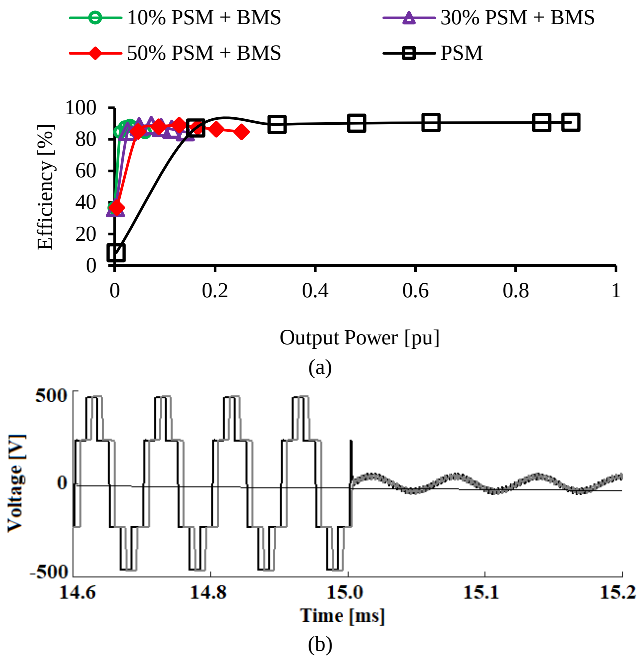


Fig. 11: AC voltage waveforms of phase A in bridge 1 and 2 (a) Within one cycle of BMS (m = 30%) at V_b = 700 V (b) Time-expanded waveform of (a).

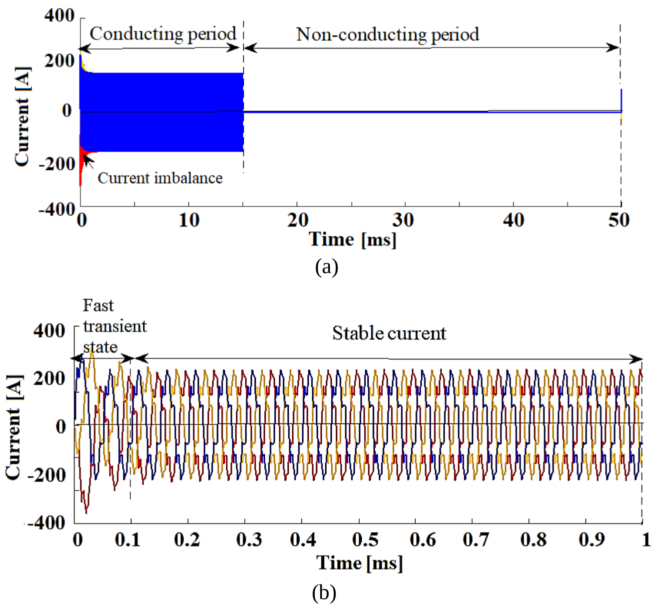


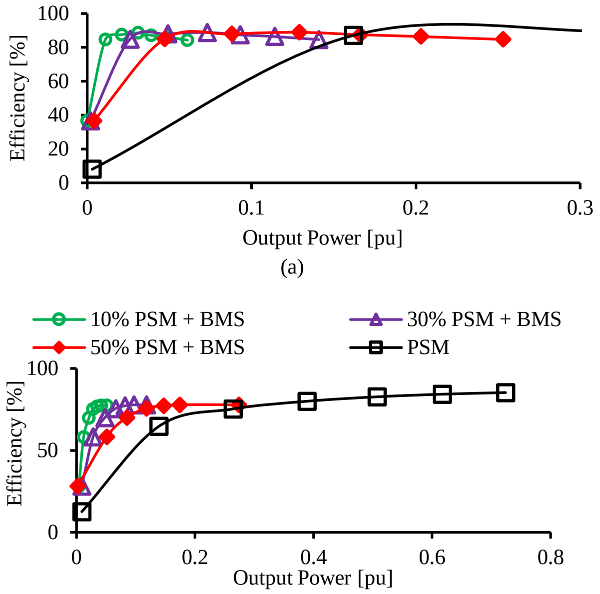
Fig. 12: Inductor current waveforms at δ=30°, $V_1 = V_b$ = 700 V. (a) Within one cycle of BMS (m = 30%) (b) Time-expanded waveform of (a).

is impractical. The maximum output power achieved at $\delta = 30°$ is when 525 V and 350 V is 0.724 pu and 0.490 pu respectively.

5.2. Combination of Phase-Shift Modulation and Burst-Mode Switching

Figure 11 (a) shows the AC voltage waveform when *m* is set at 30%. The switching occurs for 300 complete cycles and goes through a non-conducting state after 15 ms. Figure 11 (b) shows the last four cycles out of the 300 cycles at the transition from the conducting state to the non-conducting state. It is confirmed that the waveforms are similar to the waveforms obtained in PSM technique except that the cycle is not continuous and oscillates as long as the duration of *m*.

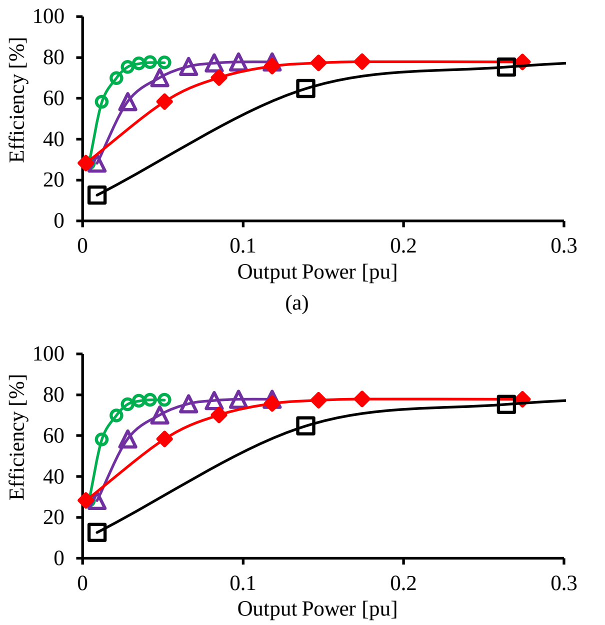
Figure 12 demonstrates the three-phase inductor current waveforms when the low-frequency signal is set to 30%, the inductor current



(a)

(b)

Fig. 13: Comparison of efficiency versus output power (a) between PSM and BMS ($m = 10\%$, $m = 30\%$, and $m = 50\%$) when $V_b = 700$ V and $0 \leq \delta \leq 30°$ (b) Time-expanded efficiency curve of (a).



(a)

(b)

Fig. 14: Comparison of efficiency versus output power (a) between PSM and BMS ($m = 10\%$, $m = 30\%$, and $m = 50\%$) when Vb = 525 V and $0 \leq \delta \leq 30°$ (b) Time-expanded efficiency curve of (a).

flows in the converter for 15 ms. As shown in Figure 12 (b), the setting time for inductor current transient is 0.1 ms.

Figure 13 presents the relation of the converter efficiency with change in output power at $V_1 = V_b = 700$ V. It is shown that when BMS with conduction duration of 10%, 30% and 50% is combined with PSM, the efficiency of the converter is improved significantly. At the output power of 0.1 pu, the converter efficiency increases by 27% when $m = 50\%$. Figure 14 (b) shows the time expanded efficiency curve. As the output power becomes lower, less than 0.028, different conduction period results in different converter efficiency. At the output power of 0.028 pu, it is shown that, when BMS with $m = 10\%$ is applied, the converter efficiency is 88.5%. However, when BMS with $m = 50\%$ is applied, the converter efficiency is 65%.

Figure 14 presents the relation of the converter efficiency with change in output power at $V_1 = 700$ V and $V_b = 525$ V. It is shown that when BMS with conduction duration of 10%, 30% and 50% is combined with PSM, the efficiency of the converter is improved significantly when the output power is less than 0.16 pu, the converter efficiency is increased by 27% when $m = 30\%$. Figure 15 (b) shows the time expanded efficiency curve. Similar to Figure 13, there are differences in converter efficiency as a result of varying conduction period. At the output power of 0.028 pu, it is shown that, when BMS with $m = 10\%$ is applied, the efficiency is 75.3%. However, when BMS with $m = 30\%$ is applied, the efficiency is 58.3%.

6. Conclusion

This paper discusses the design and operation of a three-phase bi-directional isolated dc-dc converter (3P-BIDC). In particular, it presents an enhanced switching strategy that combines phase-shift modulation and burst-mode switching for low-load operation of the 3P-BIDC. The dc-dc converter model and enhanced switching strategy are verified via a simulation. The proposed switching strategy is shown to be effective in improving the dc-dc converter efficiency at low-load conditions with the conduction period *m* as the main controlling variable and the BMS frequency fixed at 20-Hz. It is observed that different conduction period may result in varying the efficiency improvement levels. For future work, the operation and efficiency improvements will be verified via an experimental setup.

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