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Research paper

Performance Analysis of Multilevel Inverter for Different Pulse with Modulation Techniques

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Abstract

This paper introduces Multi-level inverter with different Modulation Technique. Due to major advantages Cascaded H-Bridge Multi-level Inverter is presented in this paper. Performance of Cascaded H-bridge Multi-level Inverter with Sinusoidal Pulse Width Modulated (SPWM) and Space Vector Pulse Width Modulated (SVPWM) has studied and compared their simulation results and FFT Analysis. Depending upon the carrier signals used in SPWM technique, it is sub divided into four types there are explained in this paper. The SVPWM technique used in this paper generate the switching signals directly from reference vector without using look up tables. The proposed SVPWM method can be used for any n-level inverter. Simulation results of 3-level and 5-level inverters with SPWM and SVPWM techniques are presented in this paper

Keywords: *Renewable hybrid system; Bidirectional buck/boost converter; transformer coupled bidirectional boost dual half bridge converter; Maximum power point tracking; Battery management system.*

1. Introduction

All multilevel inverter fed variable AC drives are finding more significance in many industrial applications. Due to reduced harmonic performance and less stress on the switching devices [1][2][3][4]. It gives variable Frequency and variable Voltage for control of drive applications [1]. Multilevel inverters offer output Voltage with small common mode voltage; operate at low switching Frequency and low du/dt [2]. They are three differ- ent multilevel inverters topologies which are Cascaded H-Bridge, Diode Clamped Inverter and Flying Capacitor Inverter. In pro- posed work Cascaded H-Bridge Multi-level Inverter is considered because of its advantages [3].

There are different PWM techniques, among these tech- niques we consider SPWM and SVPWM techniques for proposed work[6-8]. The SVPWM technique is an advanced and best one among the PWM techniques because of better DC bus utilization, low harmonic distortion, reduced switching losses and easy digital implementation [4]. In the present work, SVPWM technique is implemented without use of look up table. The proposed technique is based on the study that one of the switching states is at zero level among the three switching states in each of three 120 degree region. This observation also used to get the simple relation between switching states and the coordinates of instantaneous reference vector. The duration of gating signals are calculated from volt-sec balance principle. The proposed scheme has benefit of reducing complexity that is entire algorithm are based on integer values only. The SVPWM method using Cartesian coordinates which includes fractional coordinate which leads to

increase complexity. In proposed scheme one of the switching state is at zero level therefore the whole switching coordinates are used only integers

This paper is planned as follows, Section II introduces Sinusoidal Pulse Width Modulation (SPWM). Space vector Pulse Width Modulation (SVPWM) is explained in Section III. Simulation results on a proposed SPWM and SVPWM are provided in Section IV. Finally last section draws the conclusions.

2. Sinusoidal pulse width modulation (SPWM) for MUTI- level inverter

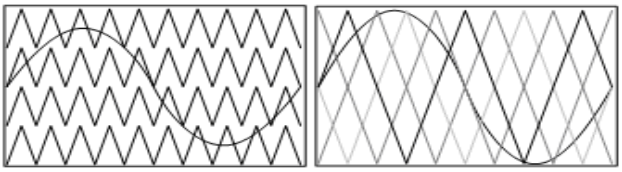
As in proposed work Cascaded H-Bridge Multi-level Inverter uses Sinusoidal Pulse Width Modulation (SPWM) technique. It is a carrier based type of Pulse width Modulation. By using PWM technique we generate high frequency pulse and low frequency output signal.

This method is simple and easy to implement when com- pared with other techniques. The pulses are generated by comparing the reference Sinusoidal signal with several Triangular signals. The multiple number of pulses are of different width are generated and width of each pulse is varying in proportional to amplitude of Sinusoidal wave.

For N- level Multilevel Inverter N-1 carrier signals with Amplitude A_c, one reference signal with A_m are used.

Amplitude Modulation Index is given by

$$M = \frac{V_m}{V_c} \quad (1)$$



1(a) 1(b)

Fig. 1: (a) vertically and (b) Horizontally shift carriers

And the carrier signals used in Multi-level Inverter might be horizontally shifted or Vertically shifted as exposed in figure.[1] The vertically shifted carriers method is simply implement on any digital control and this scheme is further divided into three types as shown in figure. 2 (a), (b) and (c)

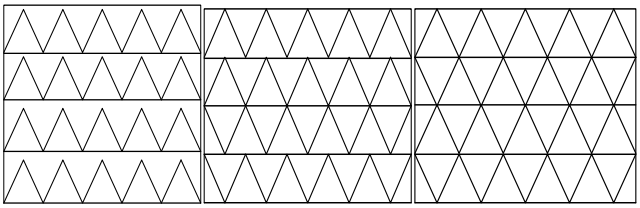


Fig .2: (a) PH (b) PO (c) APO

(a)PH disposition
(b) PO disposition
(c) PO disposition

2.1. SVPWM without Using Lookup Table

The Fig.[3] describes the coordinates of 5-level Inverter volt- age vectors. The coordinates (VM ,VN) are divided into 600– degrees framework. In this paper integer coordinates of voltage vectors are considered by neglecting the fractional coordinate. The vector coordinates are obtained from the scaling of (VA ,VB ,VC) reference phase voltage. When considered space vector diagram it is observed that reference vector tip is surrounded by four vectors (which form a parallelogram). The main work of proposed scheme is to identify the three adjacent vectors (among four vectors) and switching in suitable timings. The switching states of 5-Level Inverter is show in Fig.[4], it is separated into 3- segment, seg- ment-1, segment-2, and segment-3. And each segment of 1200

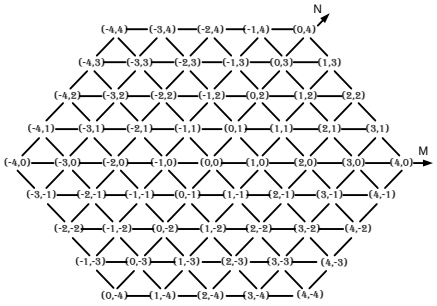


Fig.3: Coordinates of 5- level inverter in M-N Sixty degrees

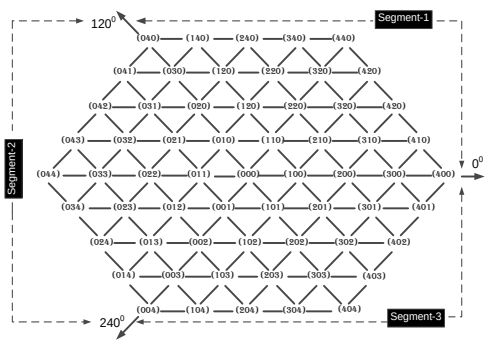


Fig.4: Switching states of five level inverter

Let SA ,SB and SC indicate the switching states of 3- phase Multi-level Inverter. If we observe the switching states of 5-Level Inverter (Fig.4), among form the three switching states one state is at '0' level in three segments. That is SA ,SB and SC are at '0'Level in segment-2,segment-3 and segment-1 respectively. Table.1 gives the relation between the switching states (SA, SB, SC) and coordinates of Inverter vectors (m, n) in the entire three seg- ments.

Table I: Relation between the switching states (S_A, S_B, S_C) and coordinates of 5-Level Inverter vectors (m, n)

segment	*Three phases Switching States*		
	S_A	S_B	S_C
1	$m+n$	n	0
2	0	$-m$	$-(m+n)$
3	n	0	$-n$

Depending on the distance between the three vectors and reference vector are named as first vector, second vector and third vector. The durations of these three vectors are T1, T2, and T3 respectively and they are determined by using volt-second balancing principle. TGA , TGB and TGC are gating signals of phases A,B and C respectively and there are determined from duration of three vectors. The general expression of gating signals duration is given in equation (2)

$$DGA = [1 + (m* - m) + (n* - n)] \quad (1)$$

$$DGB = [1 - (m* - m) + (n* - n)] \quad (2)$$

$$DGC = [1 - (m* - m) - (n* - n)] \quad (3)$$

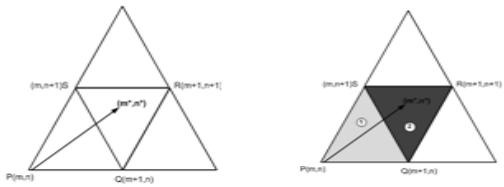
2.2 Identifying Three nearest Vectors of Parallelogram

Let the reference space vector coordinates be m* and n* in the 600 coordinate region which are obtained from

$$m^* = V_A - V_B \quad (4)$$

$$n^* = V_B - V_C \quad (5)$$

Where VA, VB, VC are the reference of 3- phase voltage amplitudes. It is observed form Fig .5(a) that reference vector lies in the parallelogram which is formed by the four vectors situated at P, Q, R and S. The proposed work directly determine the coordinates of the vectors situated at P, Q, R and S from (m, n) coordinates and these coordinates are obtained from the reference coordinates (m*, n*).



5(a) 5(b)

Fig.5 (a), (b): Identifying the coordinates of parallelogram and triangle from reference vector

The coordinates of the vector at P, can be directly determined from the instantaneous reference coordinates (m*, n*).

$$m = \text{floor}(m^*) \quad (17)$$

$$n = \text{floor}(n^*) \quad (18)$$

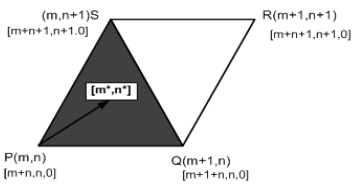


Fig. 6: Three vectors located closest to the instantaneous reference space vector from among the four adjacent inverter voltage vector

From (m, n), the coordinates of three vectors, located at Q, R and S can be determined as (m+1, n), (m+1, n+1) and (m, n+1) respectively using incremental operations. The three nearest reference space vectors are selected among from the four adjacent vectors, located at P, Q, R and S. Form Fig. [6] it is observed that along the line QS, the sum of the coordinates of Q and S is m+n+1.in proposed plane this sum is used as a reference to identify the three vectors located nearest to the tip of the instantaneous reference space vector.

If m* + n* < (m+n+1)

Then reference vector lies in region (1), as shown in Fig.5(b) and the three nearest vectors are located at P, Q, and S having coordinates as (m, n), (m+1, n) and (m, n+1) respectively.

Else, if m* + n* > (m+n+1)

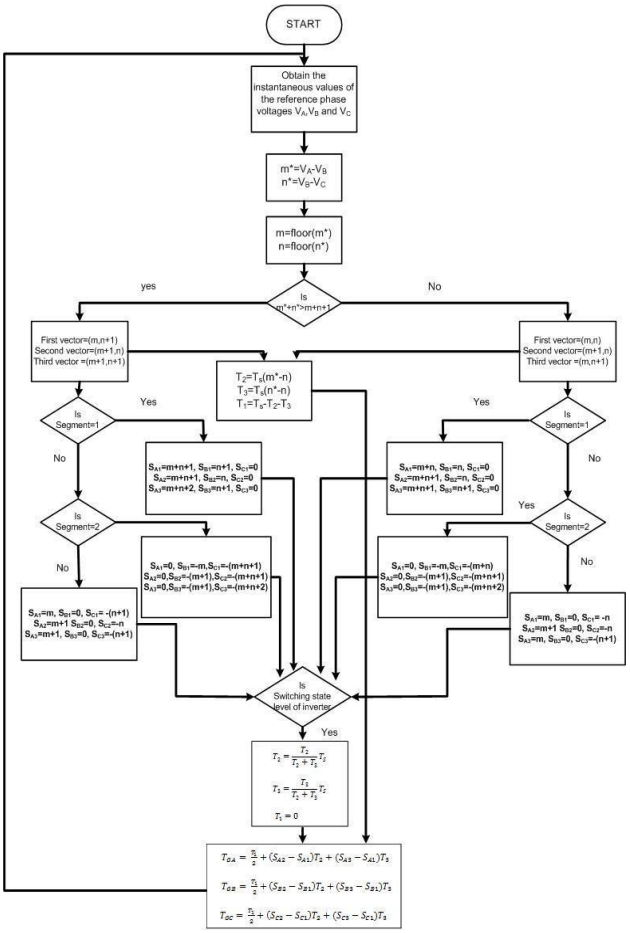
Then reference vector lies in region (2),as shown in Fig.5(b), and the three closest vectors are Q, S and R with coordinates as, (m+1, n), (m, n+1) and (m+1, n+1) respectively.

2.2.1. Over Modulation

The maximum possible switching state are 'n-1'for an 'n' lev- el inverter. Hence we can identify over modulation by examina- tion the presence of 'n' in the switching state of the vertices. In the situation of over modulation, we need to switch only two vectors, which in the present plane we named it as second vector and third vector. The timings of the second vector and third vector are determined using volt-second balance equations. Therefore in over modulation, the durations T2 and T3 are modified to T1-OVM and T2-OVM

$$T_{first\_OVM} = \frac{T_2}{T_2+T_3} \times T_S \quad (19)$$

$$T_{second\_OVM} = \frac{T_3}{T_2+T_3} \times T_S \quad (20)$$



The flow chart describe the step by step process of generating gating signals in SVPWM, without use of look up table for any n-level inverter.

3. Results and analysis

Fig .7 (a) and (b) describes the output phase voltage wave- form and THD result of 3-level Cascaded H-Bridge with SPWM technique

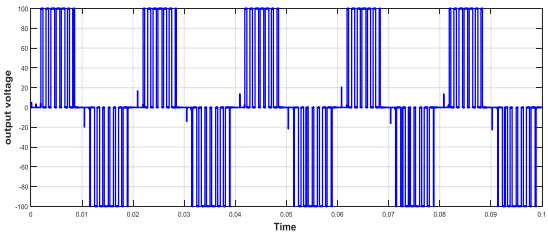


Fig.7 (a): 3-level inverter output phase voltage

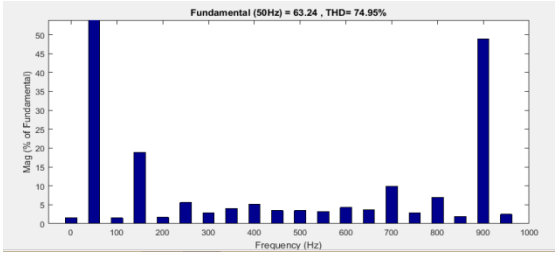


Fig.7 (b): 3-level inverter THD Analysis

Fig .8 (a) and (b) describes the output phase voltage waveform and THD result of 3-level Cascaded H-Bridge with SVPWM

technique

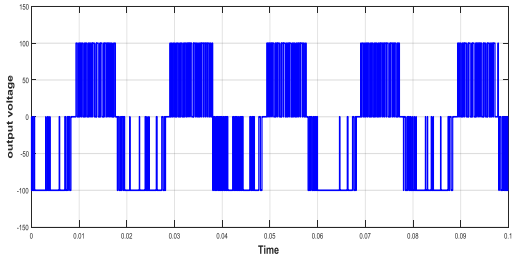


Fig.8 (a): output voltage of 3-level inverter using SVPWM

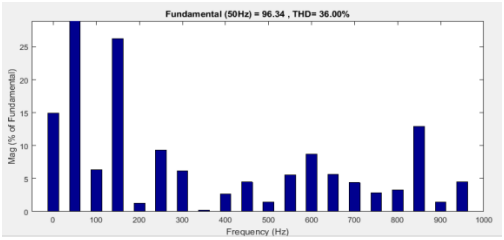


Fig.8 (b): THD of 3-level using SVPWM

Fig .9 (a) and (b) describes the output phase voltage waveform and THD result of 5-level Cascaded H-Bridge with SPWM technique

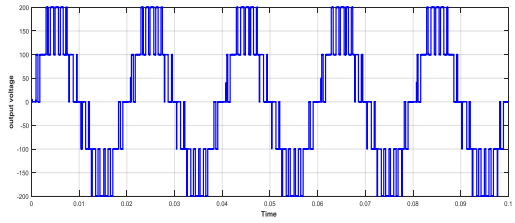


Fig.9 (a): 5-level output phase voltage using SPW

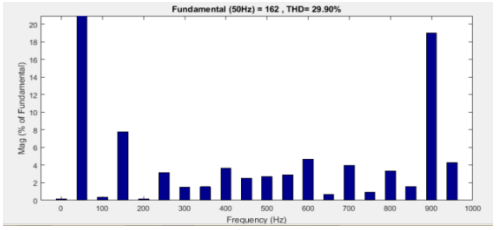


Fig .9 (b): THD of 5-level using SPWM

Fig .10 (a) and (b) describes the output phase voltage waveform and THD result of 5-level Cascaded H-Bridge with SVPWM technique

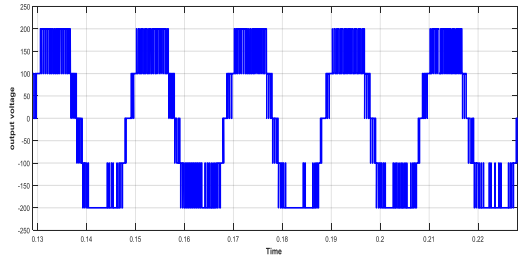


Fig.10 (a): 5-level output voltage using SVPWM

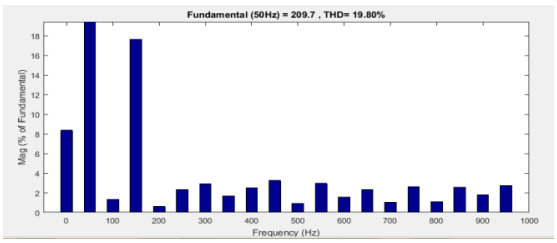


Fig.10 (b): THD of 5-level using SVPWM

Table II: Comparison of Output Voltage THD values of SPWM & SVPWM

Modulation Index	SPWM		SVPWM	
	$3-Level$	$5-Level$	$3-Level$	$5-Level$
1	74.95%	29.90%	36.01%	19.80%
0.9	81.26%	33.45%	38.24%	23.14%
0.6	112.32%	49.30%	69.10%	33.22%

Table III: Fundamental Output Voltages of SPWM & SVPWM

Modulation Index	SPWM		SVPWM	
	$3-Level$	$5-Level$	$3-Level$	$5-Level$
1	63.24	162.32	96.34	209.7

4. Conclusion

The simulation results of SPWM technique and SVPWM technique are compared. From the results and analysis it is ab- sorbed that THD content of output voltage is less in the SVPWM when compare with SPWM. The Table II and Table III compare the THD of output voltage and fundamental voltage. It is observed that SVPWM utilize 15% more dc bus when compare with the SPWM. It was conclude that SVPWM technique is more suitable than SPWM technique.

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