International Journal of Engineering & Technology, 7 (4.6) (2018) 583-585

International Journal of Engineering & Technology

Website: www.sciencepubco.com/index.php/IJET

Research paper

Investigation on Low Power for Reducing Counter Delay Digital Circuit Using 45nm Technology

[1] *Mr.S.Mohamed Sulaiman ,[2] Dr.B.Jaison , [3] Dr.M.Anto Bennet, [4] S.Purushoth, [5] R.Jawahar, [6] T.Suriya

[1]Asst.Prof, [3]Professor[3-6]UG Students
[1,3,4,5,6,]Department of Electronics and Communication– VEL TECH , Chennai 600002
[2]Associate Professor,Dept of CSE ,RMK Engineering College,Chennai
**E-mail: mohamedsulaiman@veltechengg.com,*

Abstract

The counter circuit is a basic component in floating point operation. The main aim is to speed up the operation of the circuit. The new derived Boolean function which is designed by the concept of transmission gate logic in order to reduce the number of gates and speed the circuit operation. By the transmission gate logic the 8 bit counter circuit is designed. Moreover, 16 bit and 32 bit circuit is designed using 45 nm technology. The result of 16 and 32bit circuits are better than the reported design and by comparison, proposed design is faster and the delay of the circuit is minimized when compared to the reported design.

Keywords

1. Introduction

The counter circuit is an essential element in floating point operation The design is to increase the speed by reducing the delay . So there is a research for increasing the speed and also some investigation is needed about it. By the investigation ,the concept of transmission gate logic is suggested to design circuit using 45 nm technology in cadence virtuoso software. The transmission gate logic is also one of the concept in the CMOS design . The transmission gate logic is used for reducing the number of transistors and also used to increase the speed of the circuit in order to show the best performance[5-7].

2. Principle and design of counter circuit

The 8bit circuit consist of 8 inputs (A7,A6,A5,A4,A3,A2,A1,*A*0) and four outputs (V,X2,X1,X0).The 16 bit also consist of two 8 inputs and 5 output (V,X3,X2,X1,X0).Then 32 bit also consist of four 8 inputs and 6 outputs (V,X4,X3,X2,X1,X0).The 16 bit and 32 bit circuit is designed on transmission gate logic. Due to this speed of the circuit is increased. The circuit consist of NOR gate, or gate, AND gate, NAND gate and NOT gate. By the 8bit design the outputs are given as a Boolean expressions,

$$G0=\overline{(A7+A6)} \quad ,G1=(A7+\overline{(A6.A5)}) \; , \; G2=\overline{(A5+A4)} \; , \; G3=A4+A6 \tag{1}$$

$$G4=\overline{A3+A2} \quad , \; G5=(A3+\overline{(A2.A1)}) \; , \; G6= \; A1+A0 \; , \; H0=\overline{(G0.G2)} \tag{2}$$

$$H1= \; \overline{G0}.(G2+\overline{G4}) \quad , \quad H2=\overline{G1.(G3+G5)} \quad , \quad H3=\overline{G4.G7} \tag{3}$$

$$\mathbf{V=H0+H3 \; , \; X0= H0, \; X1=H1 \; , \; X2=H2} \tag{4}$$

These are the Boolean expressions from the 8bit architecture. If the inputs of 8bit are A7,A6,A5,A4,A3,A2,A1,*A*0 =11110000 the output was 1111 . Then the inputs are A7,A6,A5,A4,A3,A2,A1,*A*0 =10101010 the output was 1100. The circuit is designed to represent the output in the form of binary. If all the 8 inputs are zeros then the output was 0011 in 8 bit architecture. This shows that all the variation of inputs is giving the at least one output as 1. So this shows that the system is better in operation and performance of the design[1-4].

3. Proposed system

The 8bit,16 bit, 32 bit architecture of was given below. The below 3 architectures are designed using transmission gate logic which is shown in the Fig:2,4,6. By the TG logic the number of logic gates have been reduced which increase the speed of the circuit. The delays of the circuits are varies. The 8 bit RCD circuit is designed of simple logic gates such as NOR, OR, NAND, AND, Inverter.

The outputs equations of the 8 bit circuits are,

$$V = \overline{(A7+A6).(A5.A6)}+\overline{(A3+A2).(A1+A0)} \tag{5}$$

$$X0= \; \overline{(A7+A6).(A5.A6)} \tag{6}$$

$$X1=(A7+A6).(\overline{(A5+A4)} + (A3+A2)) \tag{7}$$

$$X2=((A7+A6.A5).(\overline{(A2+A4)})+(\overline{(A2.A1)+A3})) \tag{8}$$

These are the simplified equations from the design. The longest path of the circuit is been simplified which increase the speed of the circuits and also the performance.

The 8 bit has an 8 inputs which are given as(11110000). Finally the output of the 8 bit was 1111.This shows the 8 bit design performance was better in showing the output. The output of the 8bit is shown in the Fig:4&5. The 16 bit also given as the inputs as(11110000). The output of the 16 bit was shown in the Fig:6&Table 7 and also the output of 32 bit was shown in the Table 89. The proposed system was given in the conclusion. The conclusion of the proposed design shows the better performance in the logic of transmission gate logic.

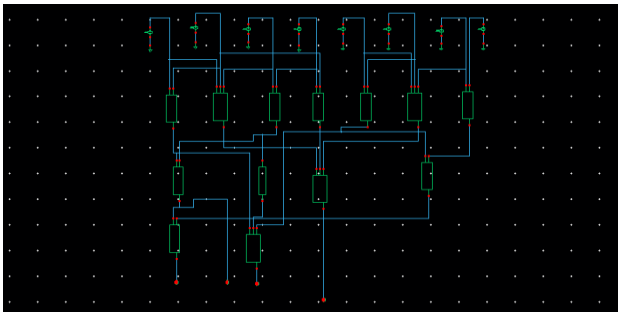

Figure 1 : 8bit Architecture

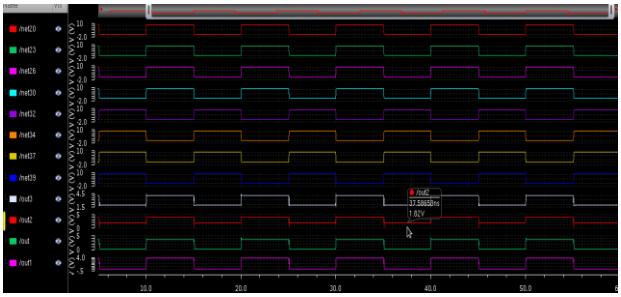

Figure 2 : 8bit Output

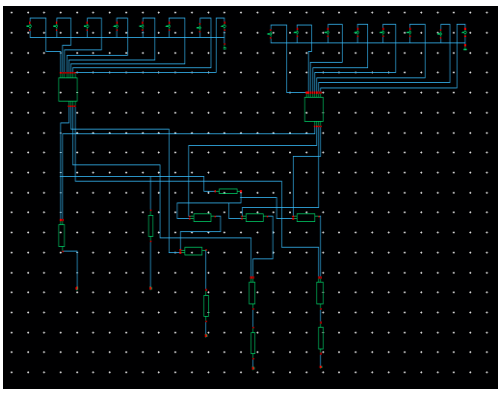

Figure 3 : 16 Bit Architecture

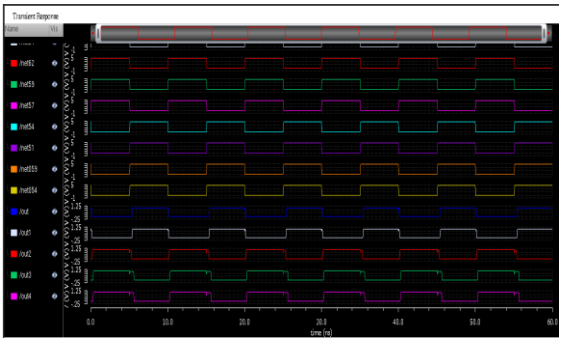

Figure 4: 16 Bit Output

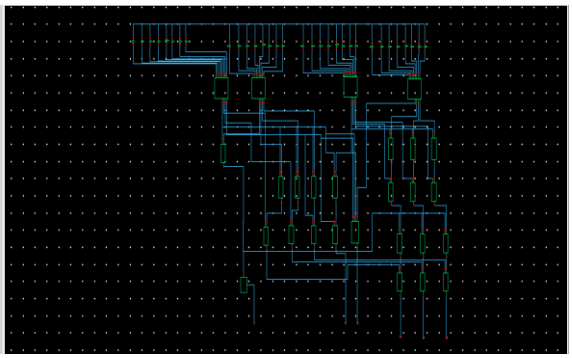

Figure 5 : 32 Bit Architecture

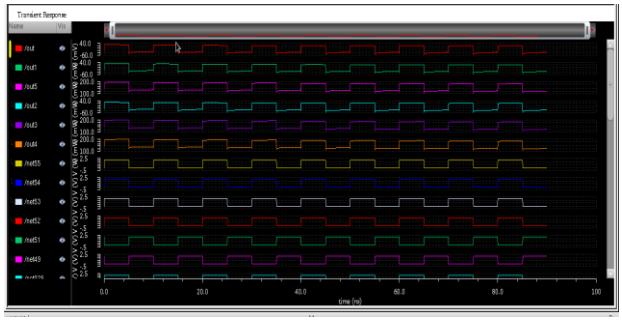

Figure 6 : 32 Bit Output

4. Experiment result:

The 16 bit and 32 bit architectures using transmission gate logic has shown the best performance of reducing the delays which are given below the table.

Table 7 : Comparison of delays between conventional design and proposed design

Devices	16bit delay	32bit delay
Conventional design[1]	14.293ns	0.512ns
Proposed design	0.0188ns	0.15ns

Table 8 : Comparison of power consumption between conventional design and proposed design

Devices	16bit power consumption	32bit power consumption
Conventional design[4]	52.00mW	65.85mW
Proposed design	1.623mW	0.3342µW

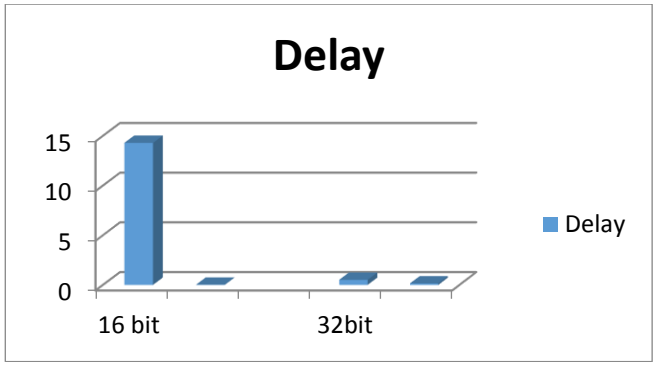

Figure 9 : Delay comparison between existing system and proposed system.

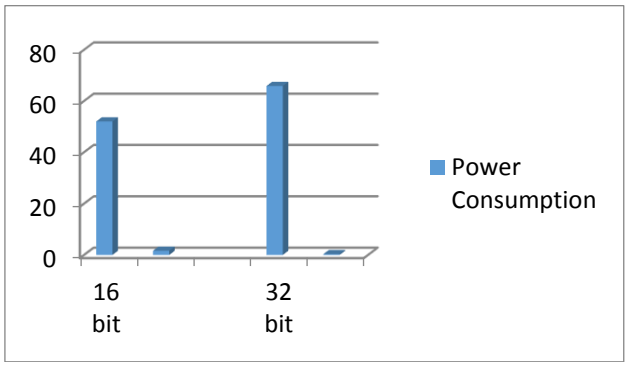

Figure 10 : Power consumption comparison between existing system and proposed system.

5. Conclusion

In our proposed design the factors like delay, power consumption are minimized by using of 45nm technology. The power consumption 16bit and 32bit design is reduced to **88.15%** and **49.24%**. The delay of 16bit and 32bit was reduced to **87.45%** and **70.7%.** The result of delay and power consumption of proposed design shows the better performance than the conventional design.

Reference s

[1] J. Miao and S. Li, "A design for high speed leading-zero counter," 2017 IEEE International Symposium on Consumer Electronics (ISCE), Kuala Lumpur, 2017, pp. 22-23.doi: 10.1109/ISCE.2017.8355536.

[2] H. Reyserhove and W. Dehaene, "A Differential Transmission Gate Design Flow for Minimum Energy Sub-10-pJ/Cycle ARM Cortex-M0 MCUs," in IEEE Journal of Solid-State Circuits, vol. 52, no. 7, pp. 1904-1914, July 2017.doi: 10.1109/JSSC.2017.2693241.

[3] S. Kumar, A. Kumar and P. Bansal, "High speed area efficient 1-bit hybrid full adder,"2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, pp. 682-686. doi: 10.1109/ICEEOT.2016.7754768.

[4] H. Reyserhove and W. Dehaene, "A 16.07pJ/cycle 31MHz fully differential transmission gate logic ARM Cortex M0 core in 40nm CMOS,"ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Lausanne,2016,pp.257-26.doi: 0.1109/ESSCIRC.2016.7598291.

[5] Dr. AntoBennet, M, Sankar Babu G, Suresh R, Mohammed Sulaiman S, Sheriff M, Janakiraman G ,Natarajan S, "Design & Testing of Tcam Faults Using T_H Algorithm", Middle-East Journal of Scientific Research 23(08): 1921-1929, August 2015 .

[6] Dr. AntoBennet, M "Power Optimization Techniques for sequential elements using pulse triggered flipflops", International Journal of Computer & Modern Technology , Issue 01 ,Volume01 ,pp 29-40, June 2015.

[7] Dr. AntoBennet, M,Manimaraboopathy M,P. Maragathavalli P,Dinesh Kumar T R, "Low Complexity Multiplier For Gf(2m) Based All One Polynomial", Middle-East Journal of Scientific Research 21 (11): 2064-2071, October 2014.