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Research paper

Performance analysis of FinFET based SRAM at nano-scaled technology nodes for low power high speed IC design

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Abstract

This paper presents the performance analysis of FinFET based SRAM in terms of delay, power and power delay product (PDP) at nano-scaled technology nodes. SRAM is generally used as memories in low powered electronics gadgets. The 85% -90% transistors of an Integrated Circuit (IC) are used to design the SRAM bit cells. As the demand for the low power high-speed devices is rising, and the emergence of Internet of Thing (IoT) devices, the need for scaled down SRAM has become essential. Since SRAM is typically constructed from traditional CMOS devices, all of the issues associated with MOSFET scaling are valid for SRAM as well. The focus of the paper is to study 6T FinFET SRAM, and evaluate the different performance metrics such as delay, power dissipation and PDP at deep-submicron technology nodes. A standard 6T FinFET SRAM cells are realized using predictive technology models (PTM) for nano scaled technology nodes. The performances of these SRAM cells are evaluated and results are compared for previously stated performance parameters. It is shown in the results that 7nm FinFET SRAM cells performs better at all aspects and followed by 10, 14, 16 and 20nm technology nodes.

Keywords: *CMOS; Delay; FinFET; Scaling; Technology Nodes.*

1. Introduction

As the popularity is rising for the low power computing gadgets and internet of things (IoT), in the modern technological era, a demand for low power electronics devices has been created with larger memory capabilities to handle the multiple processing needs. The physical sizes of the memories are constantly shrinking as per Moore's law, however, this trend cannot continue beyond a certain limit due to the physical restrictions and limitations of conventional complementary metal oxide semiconductor (CMOS) devices. [1-5]

Initially, CMOS was a promising contender for new trend of ultra-low power electronic devices. It remained there for decades before it reaching its limit. It faced many problems with scaled technologies of CMOS manufacturing process such as surface boundary scattering and parasitic. Due to reduction in the supply voltages and threshold voltage, it leads to increase the sub-threshold leakage. To tackle these issues various innovative devices have been proposed and one such device is FinFET. [6-8].

FinFET has been known to be successfully scaled upto 7nm technology node by Taiwan Semiconductor Manufacturing Company Limited (TSMC) and are being used in several embedded systems such as ARM processors, GPUs, ASIC cards, etc. This has been possible because of dramatic reduction in short channel effects and lower power dissipation of the FinFET devices. Now days, every embedded system uses some sort of memory. These memories are occupying the large area on the chip die. Hence, the performance of the systems in terms of power dissipation and speed can be affected with memory capacity and its performance. For these reasons, the memories have been an active field of study from the day of their perception. Today, a system can have two or more different types of memories. In a typical embedded or IoT system, at least two types of memory is there. The type of memory used is generally decided by the embedded or IoT system and their proposed applications. To design an embedded or IoT system, the programmer has to keep in the memory footprint of the program as the memory comes at a premium. [9-11]. The type of memory used in computing systems are volatile and non-volatile. The volatile memories loose the data when the power supply to the memory is disconnected, and non-volatile, memories that retain data without an external power source. Non-volatile memory can be classified as a secondary memory and used in USB pen drives, hard disk drives, solid state drives, etc. They are mostly used for long-term data storage. Volatile memories in contrast are referred as primary memory or main memory of a computing system. These memories are mainly used as Random Access Memory (RAM) and cache memory due to their high speed of operation for read and write cycles [12-13]. The scope of this paper is to focus on the RAM and more specifically on Static Random-Access Memories (SRAM).

This paper is organized in five sections: The brief introduction, advantages and applications of FinFET as SRAM at scaled down technology nodes are discussed in Section 1. In Section 2, the details of conventional CMOS based SRAM are discussed. Section 3 presents the circuit of FinFET based design of SRAM. Section 4 presents the evaluation results in terms of delay, power and PDP at different technology nodes. Finally, the conclusion is drawn in Section 5.

2. Static random-access memories (SRAM)

SRAM is a type of semiconductor memory which consists of a flip-flop or a latch circuit to store the data bits. Most of the flip-flops are bi-stable in nature i.e. they will store a '1' or a '0' [12-15].
A typical SRAM cell counters the drawbacks of the dynamic random access memory (DRAM). SRAM does not use the capacitors and hence they are not having complicated refresh circuit and lower power dissipation. A typical SRAM cell consists of six transistors, of which two are access transistors and rest make up the latch circuitry as shown in Fig.1.

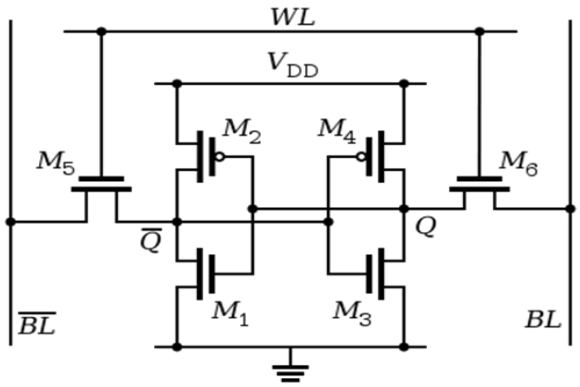

Fig. 1: An Example of A Typical 6T SRAM Cell [18].

The need of six transistors to form a cell reduces the memory density and increase the cost. Hence, manufacturers use SRAM predictably across the different computing devices depending upon the application. In most modern day computer, SRAM is fabricated alongside CPU on a single IC. [13].

3. FinFET as SRAM: need and advantages

The major challenge encountered by the semiconductor industry today is curtailing the footprint of the SRAM without negotiating on the performance to fabricate better and faster ICs since memory populates approximately 94% chip area [19-25]. Shrinking in size can occur in two ways. One is device modelling and the other is interconnects scaling. The device scaling at deep submicron technology nodes originate the many problems that are susceptible to the process variation such as variations of doping concentrations. The structures like Dual Gate Semiconductor on Insulator (DG-SOI) or FinFET can successfully replace the bulk transistors and are scalable without short channel effects (SCE) [14-15]. The schematic structure of FinFET transistor is shown in Fig. 2.

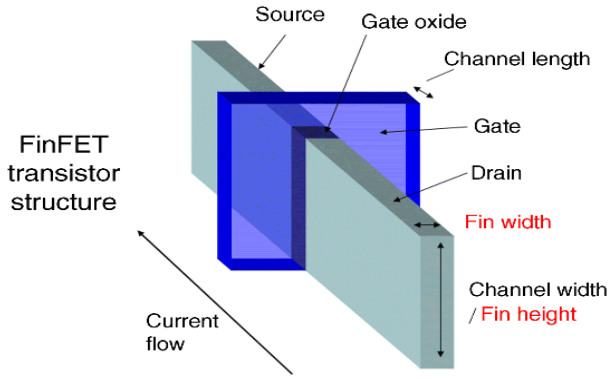

Fig. 2: The basic schematic structure of FinFET Transistor [18].

This FinFET structure consists of a thin (vertical) fin of silicon body on a substrate. The gate is wrapped around the channel providing excellent control from three sides of the channel. This structure is called the FinFET because its Si body resembles the back fin of a fish. The leakage current in FinFET is stereotypically less than that of MOSFET and has loftier scalability for a specified gate insulator thickness [16-30].
FinFET uses an intrinsic body that subdues variability in the performance of the device which are caused dopant ions concentration. Whereas, in planar bulk MOSFET, there is a stark process variability owing to the severely doped channel.

3.1. FinFET based SRAM design

FinFET has been accepted as the seemly contender for DGFET structure as shown in the previous section. (Fig. 2) [20]. Like most MOSFET devices, appropriate optimisation of FinFET devices is obligatory to lower the leakage current and upsurge the stability. For example, the leakage current in FinFET SRAMs can be reduced by optimising the supply voltage (V_D), Fin height (H_{fin}) and threshold voltage (V_{th}). This can be achieved by enlarging Fin-height, which also allows for decrease in V_D. [21]. But dropping V_D can cause stability problems and hence both parameter must be judiciously optimised. Hence, there is a compromise between standby leakage current and stability.
FinFET SRAMs are used to realise memories applications that have a need of rapid retrieval times, low power consumption and forbearance to environmental elements. Additionally, they have lowermost static power dissipation and are well-matched with prevailing logic process, which makes them quite accepted. Associated to CMOS based SRAMs, FinFET based SRAMs have higher noise margins and switching speeds [22-30].

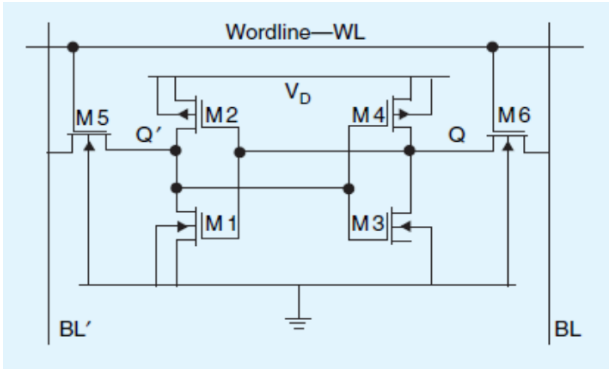

Fig. 3: Schematic of Standard 6T FinFET SRAM Cell.

The circuit design for a simple 6T SRAM cell is shown in Fig. 3. For high density memories, the cell size must essentially be small. However, the precise read process of the FinFET based SRAM cell is reliant on meticulous sizing of access transistor M5 and the pull-down transistor M1. The accurate write operation is reliant on the cautious sizing of access transistor M6 and pull-up transistor M4 as shown in Fig.3. The most critical operation in terms of complexity is the read operation from the cell. If the access transistor, M5, is miniaturised in size, then the pull-down transistor, M1, has to be fashioned big enough so that the inverter, formed by the transistors M3-M4, doesn't accidently flip its output when the voltage rises on the Q' node which inadvertently changes the bit inside the cell to '1'. After the careful selection of transistor sizes for the inverters formed by the transistors M1-M2 and M3-M4 the sizing of the access transistors M5 and M6 becomes precarious for correct operation. The threshold at which the rationed inverter (M5-M6)-M2 switches must be kept below the threshold at which the M3-M4 inverter switches so that the flip-flop formed by the inverters can switch states from Q = '0' to Q = '1'. It has been established that the performance, noise margins, and power are affected significantly by the sizing of the transistors [31-34]. Consequently, to optimise the trade-off between power consumption, performance and reliability, sizes for n-channel and p-channel FinFETs must be selected carefully.

4. Results and discussion

With reference to the discussion in the previous section, the model of a 6T SRAM cell was realized in the Tanner EDA tools as shown in Fig.4. The resulting SPICE netlist was exported to HSPICE to assess the basic read/write working of the SRAM cell. The schematic of the cell was realized using MOSFET models which were later replaced with equivalent FinFET models from Predictive Technology model (PTM) [35]. The transistors PMOS1 and NMOS1 form one inverter and PMOS2 and NMOS2 the other inverter which are cross-coupled which can be seen in the schematic. The access transistors NMOS3 and NMOS4 can be turned 'ON' or 'OFF' by the write line 'WL'. These transistors connect the inner cross-coupled inverters formed by PMOS1-NMOS1 and PMOS2-NMOS2 to the bit lines 'BL' and 'BLbar'. The layout of the 6T SRAM cell is designed in S-Edit tool and shown in Fig. 4.

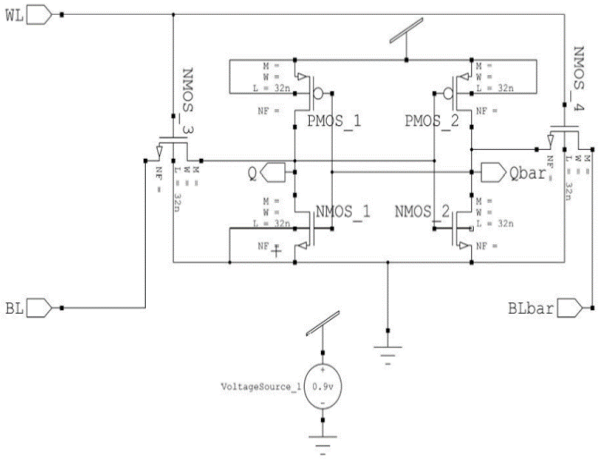

Fig. 4: The layout of FinFET based standard 6T SRAM cell in S-edit.

The evaluations were performed on 7, 10, 14, 16 and 20nm FinFET technology nodes using PTM library. All models used are low standby power (LTSP) models. The bit lines and word lines are both fed signals by pulse voltage sources. The nominal source voltage for the SRAM cell was kept at a nominal voltage of 0.9V. The pulse duration of bit line was taken as 2ns and write line pulse was taken as 20ns for all the technology nodes considered for this work.

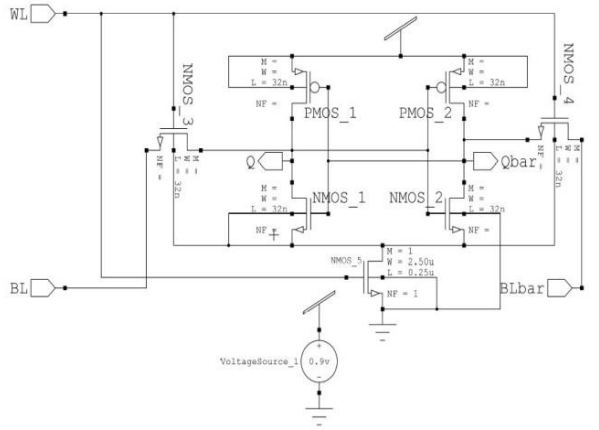

Fig. 5: Design of Finfet Based SRAM Cell with Fine Grain Power Gating.

The second circuit schematic using fine grain power gating was also modelled in S-edit tool in Tanner EDA tools, and the generated spice netlist was exported to HSPICE and shown in Fig. 5.
The various simulations parameters that had been explicitly defined in the models are provided in Table 1. All simulations were carried out with a nominal power supply, V_{dd} = 0.9V to keep the variables to a minimum.

Table 1: Simulation Parameters for Model Files

Technology Node	Fin height (nm)	Fin width (nm)	Effective length (nm)
7nm FinFET model	18	7	11
10nm FinFET model	21	9	14
14nm FinFET model	23	10	18
16nm FinFET model	26	12	20
20nm FinFET model	28	15	24

4.1. Delay and power dissipation

The designed SRAM cell is evaluated for dynamic power dissipation and the delay it takes to flip a bit inside the cell. The delay for writing '1' and '0' may differ either marginally or greatly depending upon the cell ratios, technology nodes, process variations and many other factors. The comparative analysis in terms of delay for standard SRAM cell under different technology nodes are shown in Table 2.
The bit line (BL) is initialized with a pulsating voltage source with a period of 2ns. The rise time and fall time has been kept at a realistic low value of 0.1ps so as to simulate real world delay. The output nodes 'Q' and 'Qbar' are initialized with initial conditions of '0' and '1' respectively at the start of the simulation. The word line was set with pulse period of 20ns which results in a ten write cycles, corresponding to flipping the stored data bit five times. The same conditions are used to calculate the average dynamic power over the interval from 10ns to 20ns, when the cell is active. Table 2 shows the delay and power results.

Table 2: Delay Times and Average Powers for Different Technology Nodes

Technology Node	write '1' delay (ps)	write '0' delay (ps)	Average Dynamic Power (nW)
7nm standard SRAM cell	4.107	6.137	346.9
10nm standard SRAM cell	5.126	5.749	450.8
14nm standard SRAM cell	6.155	6.443	452.4
16nm standard SRAM cell	5.064	8.323	472
20nm standard SRAM cell	8.648	12.2	303.2

The data shown in Table 2 is compiled in the form of bar graph to understand the trend of performance of FinFET memory cell in better way and shown in Fig. 6.

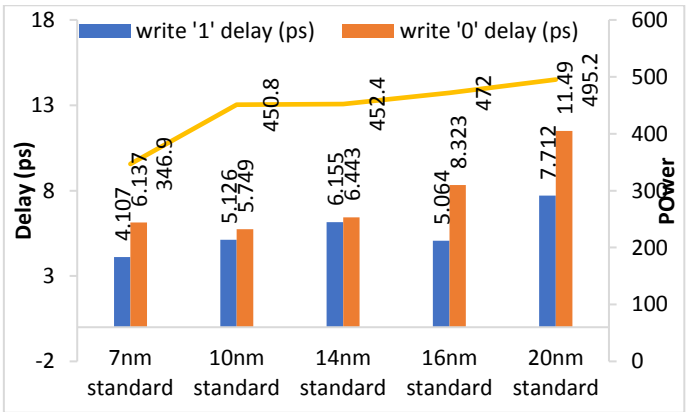

Fig. 6: Comparison of Delay and Power for Different Technology Nodes.

The graphical representation of the data gives us a clear picture of a decreasing trend in the delay times as the technology node is scaled down. However, it is interesting to observe that write '1'

delay time is always smaller than the write '0' delay. This can be attributed to the fact that the stored bit '1' has to discharge through the access transistor and word line. The cell ratio of the cell also plays a big role in defining the delay times. A lower write delay can affect the read SNM of the cell making susceptible to the data corruption while reading.

The whole process was repeated with FinFET based SRAM cell with fine grain power gating as shown in the Fig. 5. The corresponding data gathered from the above simulations is curated in a tabular form to better understand the varying trends in delay times and power dissipation and shown in Table 3.

Table 3: Delay and Average Dynamic Powers for Fine Grain Cell at Different Technology Nodes

Technology Node	write '1' delay (ps)	write '0' delay (ps)	Average Dynamic Power (nW)
7nm FineGrain	6.134	5.756	262.2
10nm FineGrain	4.895	6.314	297.6
14nm FineGrain	5.749	7.719	347.3
16nm FineGrain	5.673	9.122	375.2
20nm FineGrain	8.621	13.26	386.4

As expected, the same trend follows in terms of power dissipation and delay time, however, at 7nm node the trend slightly changes with the write '1' delay being greater than the write '0' delay. Other than that, the trend seems to be as predicted as shown in the Fig. 7.

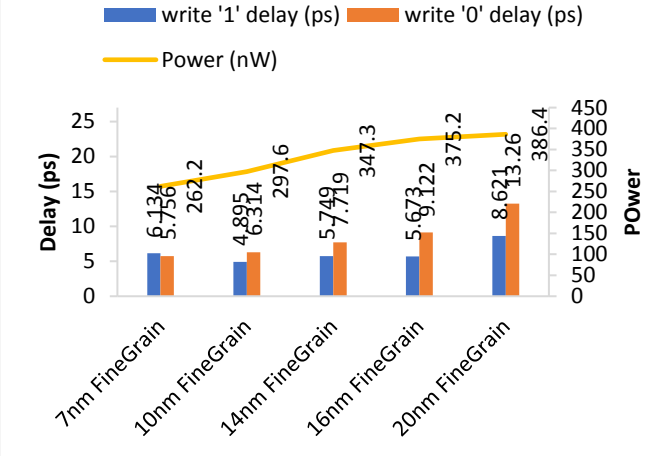

Fig. 7: Comparisons of Delay Time and Average Power Dissipation for Fine Grain Power Gating.

The average power dissipation is found to be lesser with implementation of power gating when compared to its respective technology node. The improvements in power dissipation for cells at bigger node are comparable to that of the cells at lower nodes without gating. This is one place where gating can be implemented to reduce the power dissipation without opting for lower node transistors, the fact that manufacturers have to invest a huge amount of capital while upgrading from one technology node to other. This can prove to be a kind of retro fitting option for low cost, low power applications. The delay times, on the other hand, has an increasing trend as shown in the graph.

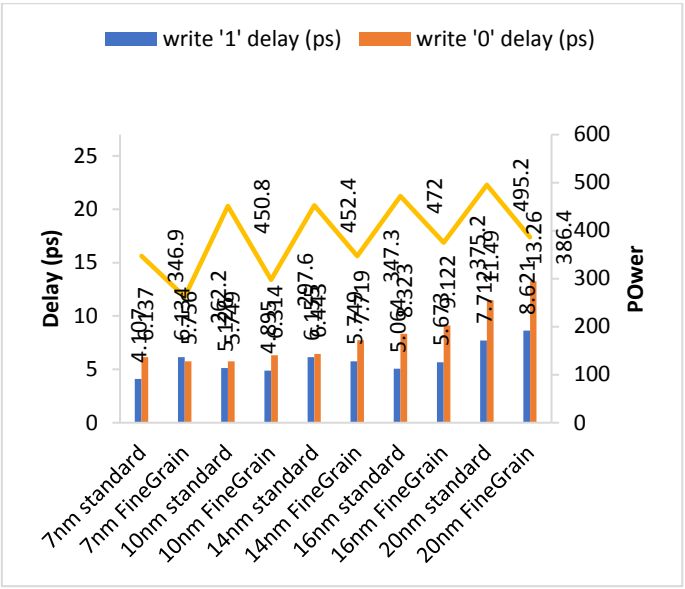

Fig. 8: Comparison between Standard Cell and Gated SRAM Cell for Each Technology Node.

It can be observed from Fig.8 that the power dissipation of 20nm fine grain cell is less than that of the standard cell SRAM at 16nm node. In fact, it is lower than all excluding the standard cell SRAM at 7nm node. It is found out that on average the fine grain cell has 24.82% less power dissipation than its equivalent standard cell counterpart.

The delay time trends aren't as straight forward as the power dissipations and may seem somewhat random. However, on a closer look it is evident that delay time is affected significantly. The average percentage increase in write '1' delay is found out to be 12.4129%. The highest reported increase in the 7nm node was with a staggering 49.35% increase in delay time. On the flip side, the lowest witnessed increase is actually an improvement with -4.51% and -6.59% decrease in delay time for 10nm and 14nm technology nodes.

The same trend follows for the write '0' delay time, with an average increase in time of 9.68% with the highest being 19.08% for 14nm node and lowest -6.20% in 7nm node, which is improvement over the standard cell. Therefore, it makes much more sense to compare the average delays rather the individual write delays. The calculated average delay times along with the power delay product (PDP) are listed in the table. The power delay profile or switching energy is correlated with energy efficiency of a logic circuit.

Table 4: Comparison of Average Power and PDP for Standard Cell and Fine Grain Cell at Various Technology Nodes

Technology Nodes	Average Power (nW)	average delay (ps)	PDP
7nm standard	346.9	5.122	1776.8218
7nm FineGrain	262.2	5.945	1558.779
10nm standard	450.8	5.4375	2451.225
10nm FineGrain	297.6	5.6045	1667.8992
14nm standard	452.4	6.299	2849.6676
14nm FineGrain	347.3	6.734	2338.7182
16nm standard	472	6.6935	3159.332
16nm FineGrain	375.2	7.3975	2775.542
20nm standard	495.2	9.601	4754.4152
20nm FineGrain	386.4	10.9405	4227.4092

The average percentage change observed in the average delay time comes out to be 10.10%. This means that cells with power gating can be expected to be 10% slower than without the power gating.

However, when power delay product is taken into consideration, the gated cells have better PDP than the cells at same technology node. The power delay should be minimum for an energy efficient logic circuit, satisfying the definition, we have the cell with power gating at 7nm node with the lowest PDP.

5. Conclusion

This paper focused on the simulation of a standard 6T FinFET SRAM cell at different technology nodes, comparing them on the basis of various parameters and successfully established an experimental proof to the theory discussed in the various sections of the paper. The SRAM cell is then power gated and compared for the same parameters. The simulation data confirm that the needs for the scaling down of the transistor for SRAM use both in terms of area and performance. It is revealed from the results that lowest PDP of 7nm FinFET SRAM is the proof for stability and efficiency combined with the lowest delay makes it ideal for embedded applications. The point to be noted is that the models used are predictive technology models (PTM) which are based on the International Technology Roadmap for Semiconductors (ITRS); hence this simulation is a proof of a concept.

Acknowledgement

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