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Research paper

Design of Low Noise Amplifier for WLAN using pHEMT

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Abstract

The low power consumption devices are frequently focused in design and manufacturing wireless communication system. This paper gives a systematic design of a low noise amplifier for WLAN application aimed to obtain minimum noise figure. The simulation result shows that the noise figure is in the appreciable level (1.67 dB). The maximum gain is greater than 10 dB. These are the predominant requirements of an LNA. Also it posses good stability and the LNA design uses pHEMT for its appreciable noise performance.

Keywords: *Impedance Matching; LNA Design; Maximum Gain; Noise Figure; PHEMT.*

1. Introduction

The design of low power devices is always suggested for wireless communication because of the limitation of portable batteries. The receivers of handheld devices are expected to consume low power and provide an optimum performance. The receiver front end consists of a low noise amplifier and a down conversion mixer. The low noise amplifier must have appreciable noise factor value (< 2dB) and gain (> 10 dB). The LNA is an essential circuit that comes immediately after the receiving antenna. It mainly manages the sensitivity of the receiver. There are various literatures presented for the design of LNA separately for the WLAN and V2V applications. This paper presents the design of an LNA operating at 2.4 GHz, for WLAN and other wideband wireless communication applications. This design holds good for the applications like WLAN, Wi-Max and vehicle to vehicle communication with its attractive noise figure property.

2. Selection of transistor and configuration

Nowadays there are numerous transistors right from BJTs is manufactured to operate at RF frequencies. The BJT in common emitter configuration or JFET in common source configuration is primarily preferred for its good stability. However common source amplifier has appreciable noise performance and can be recommended for low noise amplifier [1] design but it is high sensitive to change in bias voltage, temperature and tolerance of the components. If we go for a broad band operation in support of higher data rate application common gate configuration can be preferred. But the gain of common gate is very low. The better choice would be cascading several stages of the common gate configuration of JFET or go for cascode amplifier. The cascode amplifier is preferred for its wide bandwidth, high stability and gain. Cascoding of JFET has not so superior noise performance compared to common source amplifier. There is another option to change the device technology. The High Electron Mobility Transistor (HEMT) which has a novel PN junctions having different type of materials. Preferably the Gallium Arsenide (GaAs) or Gallium Nitride (GaN) is used as semiconductor material with different thickness and width. These materials are preferred for its high electron mobility. The HEMT are classified based on its growing technology as pHEMT (pseudomorphic HEMT) [6] and mHEMT (metamorphic HEMT). In this paper the LNA is designed with pHEMT transistor [7].

3. LNA design

3.1. Bias network

The noise figure is an important parameter of LNA determining how efficient an LNA is. The LNA must also have a high gain in order to drive the successive stages of the receiver circuitry. The LNA should provide good impedance matching characteristics with minimum components. In this paper a single stage LNA is designed using pHEMT transistor with appropriate matching networks (Fig 1). The complete LNA includes the bias network design, [2] [3] input and output impedance matching networks. The input and output of transistor and the matching network are significantly denoted by the corresponding reflection coefficient values. These are basically complex values and can be written in terms of the S-parameters of the transistor. The requirement is to produce a moderate gain with noise figure is less than 2 dB. The transistor ATF-36077 HEMT is selected for the LNA Design which has a noise figure of 0.11 dB at a bias point of V_{ds} = 3 V & I_{ds} = 20 mA.

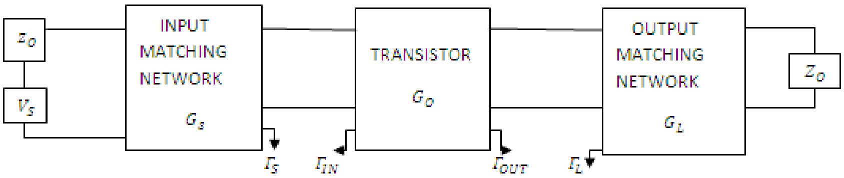


Fig. 1: Generalized LNA Design Blocks.

Stability is another important attribute of LNA which indicates the nature of oscillations present in the LNA. For a stable amplifier the oscillations won't occur at the output of the amplifier. [4] The stability is defined by two parameters they are delta and Rollet's stability factor (K). The amplifier is said to be unconditionally stable if K > 1 and |Δ| < 1, otherwise the amplifier is said to be conditionally stable which requires compensation networks. The stability factor is related with S-parameter is given by equation 1 and 2.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \qquad (1)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \qquad (2)$$

The stability can be enhanced by adding a series resistance at the gate terminal. But it would increase the noise figure because the resistor is a potential source of thermal noise. Another way of enhancing the stability is by adding an inductor at the source which significantly reduces the gain of the amplifier. There is another possibility to have a better stability is by properly designing the biasing network and impedance matching network. The biasing network is allowed to produce very small potential drop and hence a resistance of 500 Ω is added between drain and gate of the transistor [5]. The resistors 11.2 Ω is added from the 2V supply to the base and 1.2 Ω is added at the 1V supply to the drain.

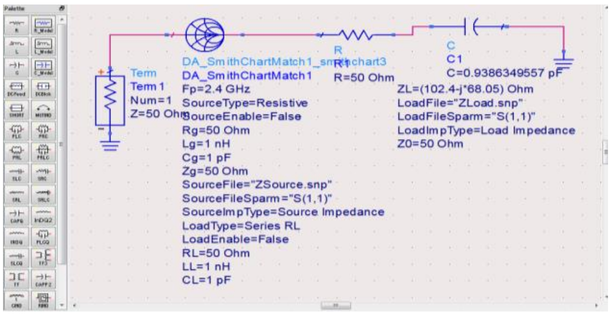
3.2. Impedance matching

The impedance matching network is designed with the knowledge of S-parameters of the transistor [9]. The input impedance matching network design requires S11 and output impedance matching network design requires S_{22} of the transistor. The typical value of S_{11} for the pHEMT (ATF-36077) at 2.4 GHz is given by −0.23+ j0.60 or 0.6425∟110.9. The input reflection coefficient is given in terms of S-parameters [10]

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L} \qquad (3)$$

Where the load reflection coefficient is given as

$$\Gamma_L = \frac{Z_L-Z_0}{Z_L+Z_0} \qquad (4)$$



```
Term
Term1
Num=1
Z=50 Ohm

DA_SmithChartMatch1_smithchart3
DA_SmithChartMatch1
Fp=2.4 GHz
SourceType=Resistive
SourceEnable=False
Rg=50 Ohm
Lg=1 nH
Cg=1 pF
Zg=50 Ohm
SourceFile="ZSource.snp"
SourceFileSparm="S(1,1)"
SourceImpType=Source Impedance
LoadType=Series RL
LoadEnable=False
RL=50 Ohm
LL=1 nH
CL=1 pF

R
R1
R=50 Ohm

C
C1
C=0.9386349557 pF

ZL=(102.4-j*68.05) Ohm
LoadFile="ZLoad.snp"
LoadFileSparm="S(1,1)"
LoadImpType=Load Impedance
Z0=50 Ohm
```

Fig. 2: Input Impedance Matching – Smith Chart Utility.

As $Z_L = Z_0$ = 50 Ω, the value of load reflection coefficient is zero, that is, output impedance of transistor and load impedance are assumed to be perfectly matched. With this condition the input reflection coefficient equals the S_{11} parameter. Further the input reflection coefficient or S_{11} is given as

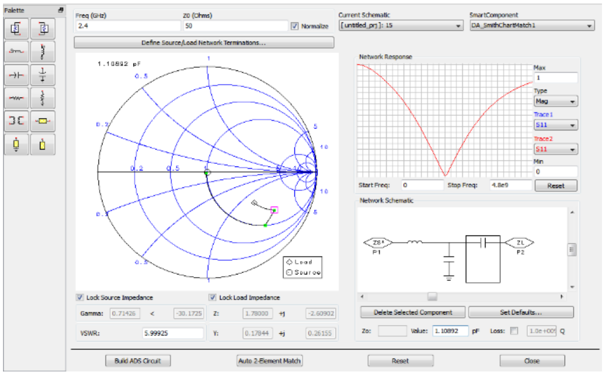
$$S_{11} = \frac{Z_{IN}-Z_0}{Z_{OUT}+Z_0} \qquad (5)$$

This equation can be modified as

$$Z_{IN} = Z_0\left(\frac{1+S_{11}}{1-S_{11}}\right) \qquad (6)$$

Substituting the values, the input impedance is found to be Z_{IN} = 1.780 – j2.6 Ω. This impedance has to be matched with 50 Ω source resistance. The impedance matching is carried out with the help of Smith Chart Utility in the ADS tool.

The input impedance is matched with a 50Ω source impedance by a T-network consists of a shunt capacitance and series LC components (Fig 3).



Freq (GHz) 2.4
Z0 (Ohms) 50
☑ Normalize
Current Schematic [untitled_prj]: 15
SmartComponent DA_SmithChartMatch1
Max 1
Type Mag
Trace1 S11
Trace2 S11
Min 0
Start Freq: 0
Stop Freq: 4.8e9
☑ Lock Source Impedance
☑ Lock Load Impedance
Gamma: 0.71426 < -30.1725
Z: 1.78000 +j -2.60902
VSWR: 5.99925
Y: 0.17844 +j 0.26155
Zo: Value: 1.10892 pF Loss: ☐ 1.0e+00 Q

Fig. 3: Input Impedance Matching Network.

The components values are calculated at the frequency of 2.4 GHz as from the source end a series inductance of 6.98512 pH, a shunt capacitance of 0.16845808 pF and a series capacitance of 1.10892 pF.

The output matching network (Fig 5) is designed by the same procedure as the design of input matching network (Fig 4). The equations governing the design of output matching is given below.

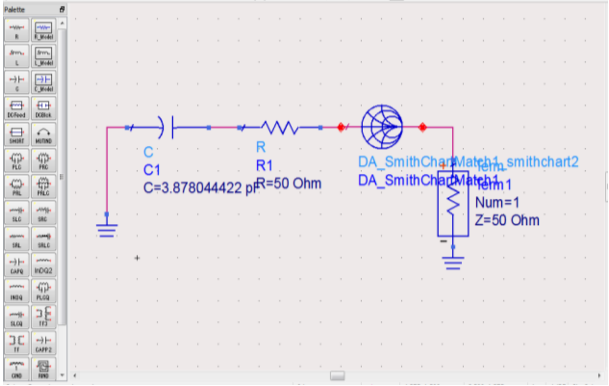


Fig. 4: Output Impedance Matching – Smith Chart Utility.

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1-S_{11}\Gamma_S} \qquad (7)$$

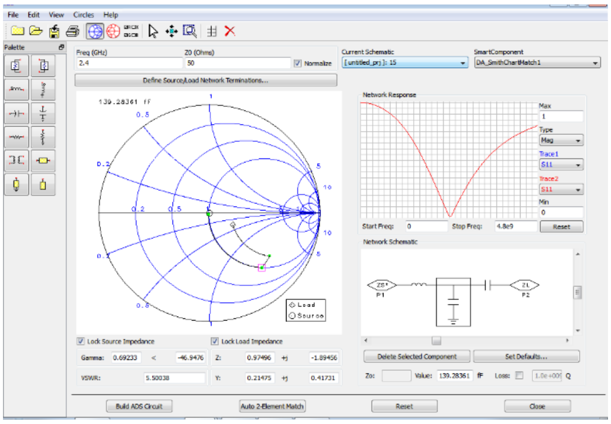
$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \qquad (8)$$

Here, $Z_L = Z_0 = 50$ ohm, as $\Gamma_S = 0$, $\Gamma_{OUT} = S_{22}$ then using

$$S_{22} = \frac{Z_{OUT} - Z_0}{Z_{OUT} + Z_0} \qquad (9)$$

$$z_{OUT} = Z_0\left(\frac{1+S_{22}}{1-S_{22}}\right) \qquad (10)$$

The value of $S_{22} = 0.21 - 0.11j$ or 0.237∟-27.65, the output impedance is calculated as 0.97 – j1.89 Ω.



Freq (GHz) 2.4
Z0 (Ohms) 50
☑ Normalize
Current Schematic [untitled_prj]: 15
SmartComponent DA_SmithChartMatch1
Max 1
Type Mag
Trace1 S11
Trace2 S11
Min 0
Start Freq: 0
Stop Freq: 4.8e9
☑ Lock Source Impedance
☑ Lock Load Impedance
Gamma: 0.69233 < -46.9476
Z: 0.97496 +j -1.89456
VSWR: 5.50038
Y: 0.21475 +j 0.41731
Zo: Value: 139.28361 fF Loss: ☐ 1.0e+00 Q

Fig. 5: Input Impedance Matching Network.

The output matching network consists of a series inductance from transistor output followed by a shunt capacitance and a series capacitance. The values of these components are given by 0.72394281 pH, 0.1392896pF and 6.17489nH respectively.

3.3. LNA circuit

In the complete design of LNA the input is connected to the gate of pHEMT transistor by using a DC blocking [8] capacitor of 1.1 pF. Output is obtained at drain with a DC blocking capacitor of 723.9 fF. Moreover the AC blocking inductances are connected between gate to supply voltage and drain to supply voltage (Fig 6). This is designed to work at 2.4 GHz.

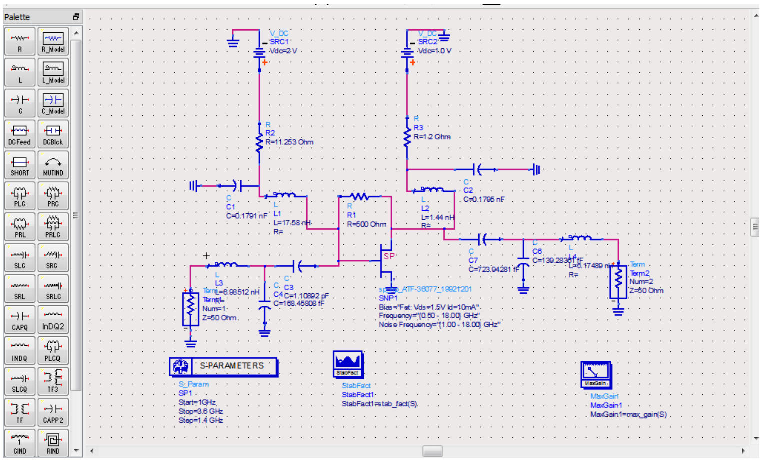


Fig. 6: LNA Circuit.

4. Simulation results

The simulation of LNA is carried out using ADS EDA tool and the essential LNA parameters like Maximum gain, available gain, noise figure and stability factor are obtained.

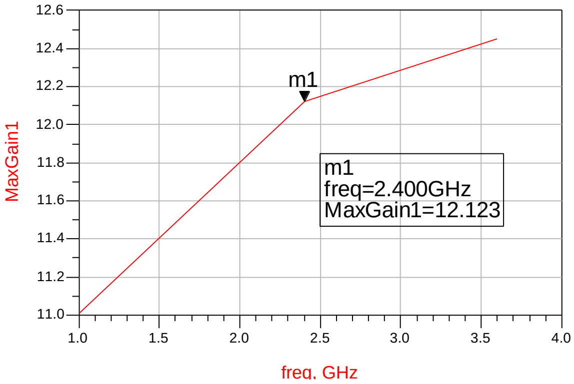


Fig. 7: Maximum Gain.

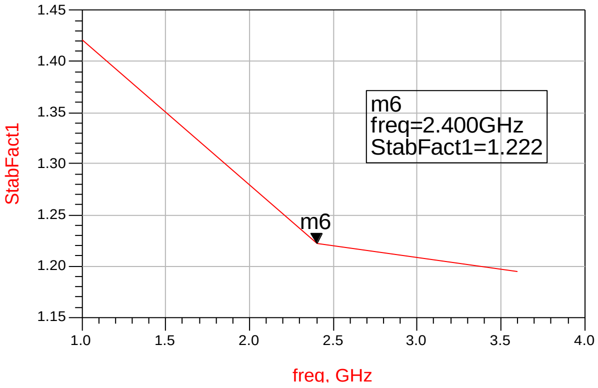


Fig. 8: Stability Factor.

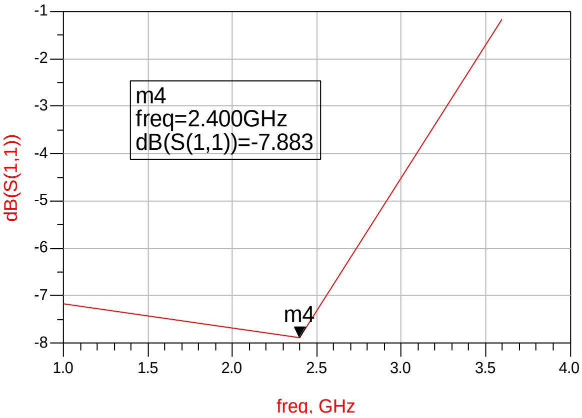


Fig. 9: Input Reflection Coefficient (S_{11}).

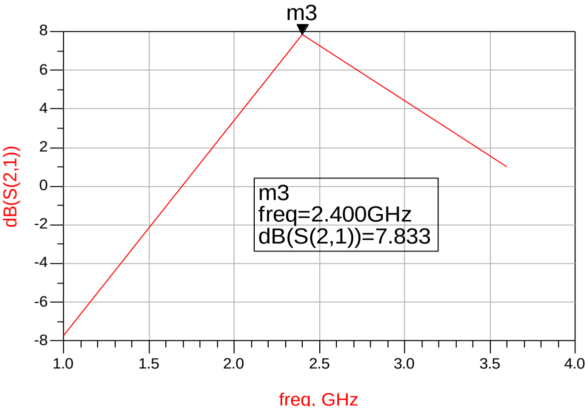


Fig. 10: Forward Gain.

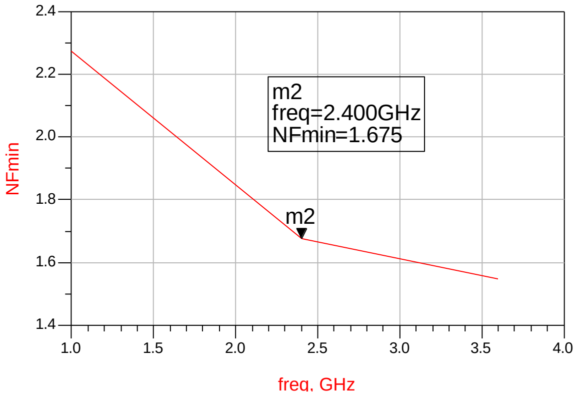


Fig. 11: Noise Figure.

From the above figures (Fig 7. through Fig 11.) the following parameters are observed at the operating frequency of 2.4 GHz. The maximum gain of 12.213 dB, stability factor of 1.22 which is greater than 1 and S_{11} is -7.88 dB. It is also observed that the S21 which corresponds to forward gain is obtained as 7.833 dB and noise figure of 1.675 at 2.4 GHz. These values assure that this is suitable for satisfied operation of LNA for WLAN applications.

5. Conclusion

The LNA is simulated using pHEMT transistor to be operating at 2.4 GHz suitable for WLAN and other UWB applications. The power consumption is very low because it has the bias voltage of 2V also the drain saturation current is 25mA. From the simulation results it is observed that the noise figure is low (< 2dB) which is suitable for front end circuitry. Also the maximum gain is obtained as around 12 dB. This basic model can be used to develop cascaded amplifiers if we desire to provide more gain with less noise figure.

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