

# Performance evaluation of heuristic algorithms in floor planning for ASIC design

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## Abstract

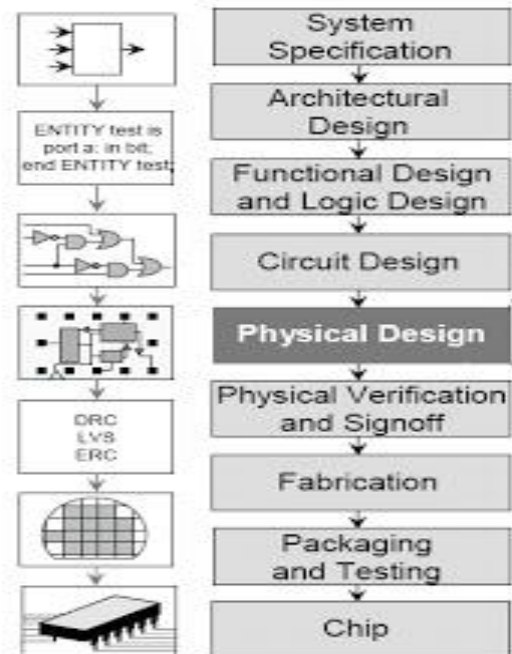
A study on physical design of VLSI Floor planning is discussed using optimization techniques for betterment in performance of VLSI chip. Floor planning in VLSI is considered to be a Non Polynomial problem. Such problems can be solved using computations. The initial step in floor plan is the representation of floor plan design. The floor plan representations show greater impact on the search space and the complexity of the floor plan design. The objective of this paper is to study different algorithms that addresses the problem of handling alignment constraints such as good placement, optimum area and short run time. Different heuristic and meta-heuristic algorithms are proposed and suggested by many researchers for solving the VLSI Floor plan problem. In this paper Simulated Annealing algorithm, Ant Colony Algorithm, Tabu search and Genetic algorithms are discussed.

**Keywords:** VLSI Floor plan, SA, Tabu search, ACO, GA

## 1. Introduction

With the rapid changes and improvements in the technology, the complexity of the design of circuits is getting increasing and the area occupying larger area hence the physical design plays a vital role in circuit designing. Physical design starts with initial step Floor Planning which should determine dimensions of blocks and locations where these blocks to be placed in a chip putting the objective of minimum area and interconnect wire lengths. The floor plan determines the size and complexity of transformation between the floor plan and its representation. VLSI Floor plan is considered to be a NP Hard problem. As number of blocks increases, it is very difficult to find optimum solution to

Fig. 1: Design Flow of VLSI circuits



VLSI meets the desired floor plan representation. The quality of floor planning depends on its representation. The figure shows the design flow of VLSI system. The design process consists of various design steps like, system specifications, architectural design, physical design, verification etc.

### 1.1 Explanation of physical design flow process

This paper mainly concentrates on the physical design process. Physical design:

In this processing stage, the geometric representations of the components like fixed shapes, sizes are assigned spatial locations and a suitable routing connections are made to achieve optimal area. As a consequence of this process, it results in a set of manufacturing specifications which need to be verified subsequently [1].

The physical design process is again divided into number of sub parts like, partitioning, Floor planning, placement, routing etc. Partitioning is a process of decomposing a circuit into several sub circuits of manageable size.

Floor plan is used to estimate size, performance, and reliability of VLSI chips. The goal of VLSI floor planning is to allocate space for the modules in such a way that no two modules overlaps with one another in the chip.

Placement step is used to assign circuit components to locations in the chip according to their geometrics. In standard cell array method of design components have same width and in macro cell design method components have different sizes and are placed invariably. The objective of placement is to mineralize the entire layout area of the chip.

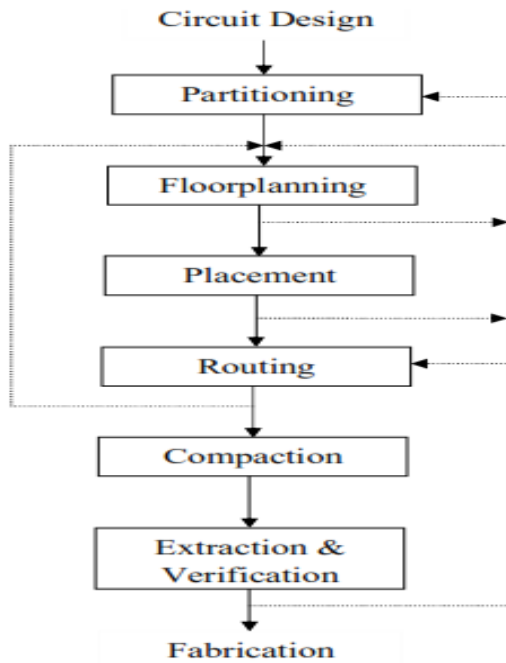


Fig. 2: Physical Design Flow of VLSI

Routing process tries to determine the way of interconnecting different modules available on the chip in terms of global and detailed routing methods.

Physical design directly shows impact on circuit performance, area, reliability, etc. for example, performance of chip affected with longer routes since long routes introduces noticeably longer delays. Area of the chip affected with the uneven placement of the components and so on.

### 1.2 Importance of Optimization

Rising technological necessities in addition to the extensive acceptance of sophisticated microelectronic devices have produced an extraordinary demand for large scale, complex, and integrated circuits. Reaching these demands required technological improvements in materials and processing equipment, noteworthy increases in the number of individuals involved in the design of integrated circuit, and an increased importance on efficiently utilizing the computer to aid in the design.

Physical design is an optimization problem which is a complex one with several different objectives such as minimizing wire-length, chip area, and Vias. Common goals of optimization are to improve the performance, reliability etc.

The process of minimizing or maximizing a function related to a set which often represents a range of options available in particular situation. Minimum cost, minimum error, maximum profit etc are some of the applications when optimization is used.

### 1.3 Overview of Existing Optimization Algorithms

Floor planning helps in determining the position/locations of the modules, in order to achieve minimum area and minimum wire-length. Different representation methods use different heuristic and meta-heuristic algorithms. Some examples of heuristic and meta-heuristic optimization algorithms are Simulated Annealing, Tabu search, Ant colony, Genetic algorithm.

### 1.4 Simulated Annealing Algorithm

Simulated annealing algorithm was proposed by Kirkpatrick, 1980's; Gellat & Vecchi between 1982 – 1983 and by Cerny in 1985. The motivation for Simulated Annealing approach is to find the optimum solution based on the correlation among the physical annealing (hardening) process of solids and the problem of solving large combinatorial optimization problem.

Annealing process involves achieving a solid's bottom state by melting it at higher temperature, and slowly lowering the temperature (annealing), particles position themselves in the ground state [4].

- First metal heating is done at a very high temperature.
- Crystal is formed as the temperature decreases.
- Higher energy state is obtained by decreasing the temperature very slowly.

The procedure of Simulated Annealing is given figure.

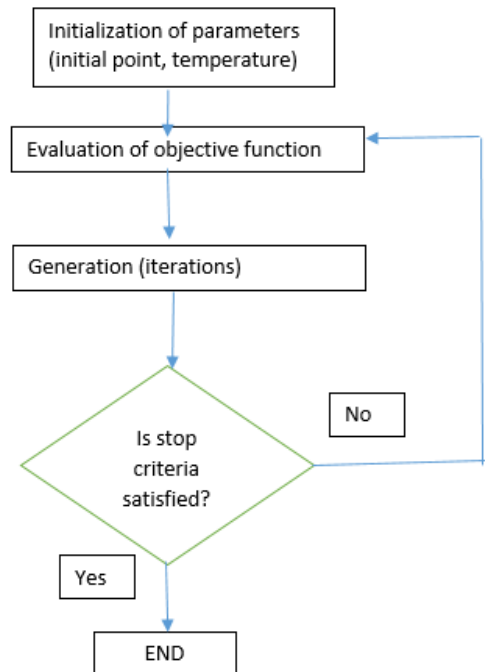


Fig. 3: Simulated Annealing

### 1.5 Tabu Search Algorithm

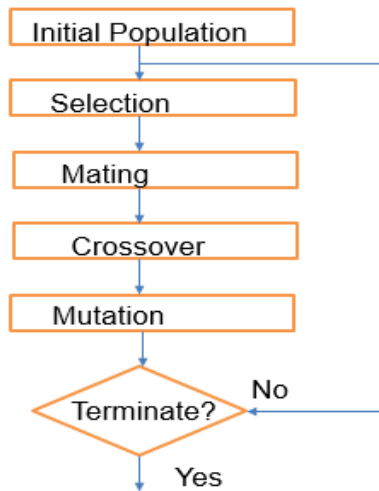


Fig. 5: Genetic Algorithm Flow Chart

Tabu search (TS) is one of the meta-heuristic approach for the problem of floor planning with non-slicing constraints. It comes into the category of iterative heuristics that are meant for providing solutions combinatorial optimization problems. It is a simplification of local search that hunts for the best change in the neighborhood of the current solution. Nevertheless, TS does not get trapped in local optima like local search since it correspondingly agree to take bad moves if they are projected to lead unvisited solutions [3].

### 1.6 Ant Colony Optimization Algorithm

Ant Colony (AC) Optimization is a population based optimization that is used to find optimum solution for complex optimization problems. The Ant colony algorithm has three stages, initialization, construction and feedback. The initialization stage involves setting up the parameters like number of Ants and number of colonies. The construction phase involves the path construction based on pheromone concentration. The feedback stage includes the extraction and reinforcement of ants travelling experiences during path searching [5].

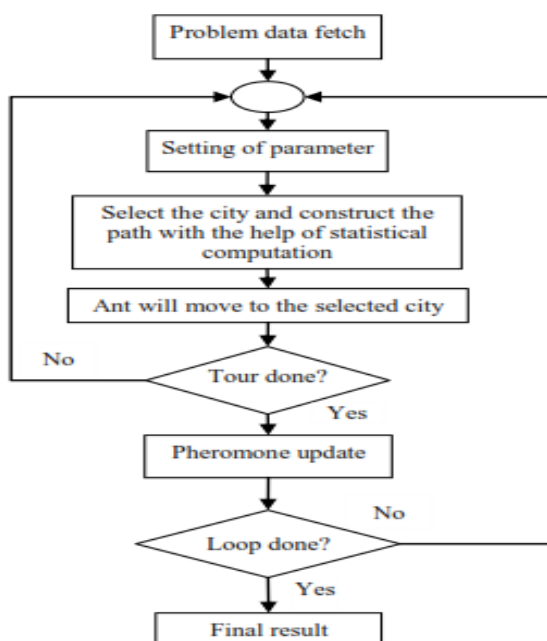


Fig. 4: Ant Colony Optimization Flow

The TSP also has a vital role in ACO search, finding the shortest distance in the middle of the Source and food. As seen in the flowchart given, initially the parameters are to be set. Select any city and construct path and ant moves to the selected city, if the distance achieved is small then stop the criteria otherwise update value and repeat the steps from setting parameters again.

### 1.7 Genetic Algorithm

The problem of achieving minimum area and minimum wire-length is solved using the Genetic algorithm. In this genetic algorithms. The working flow of Genetic algorithm is as shown below:

Genetic algorithm process flow:

- Consider the total population
- Select the best population of chromosomes
- Calculate the fitness function
- Mutation is applied to change the fitness value
- Cost calculation is done for every iteration
- If cost is minimum, then current population is treated as optimized result.
- Otherwise, this procedure continues until it gives a desired result.

## 2. Literature Survey

In 2016, k Sivasubramanian et al. [6] proposed a technique that concentrates on the reduction of area as an improvised harmony search algorithm and Twin memory Harmony search algorithm for VLSI floor planning. These two memories are initialized with HMS randomly generated. The results presented by this paper showed that the proposed algorithm THMS reduces different parameters like area, wire length, time.

In 2015, B.Premalatha et al. [7] proposed a new method for minimizing the wire length in FPGA Placement. In this, an different version of Particle Swarm Optimization algorithm called (ARPSO) "Attractive and Repulsive Particle Swarm Optimization Algorithm". In ARPSO algorithm, the updating of velocity values is carried out depending on Diversity factor D. The simulation results shows that proposed ARPSO algorithm is capable of optimized placement in FPGAs with minimal wire length.

In 2015, G Karimi et al. [8] introduced a technique for the placement of different sized modules in VLSI circuit design using "Multi Objective Particle Swarm Optimization, the author concentrated on reduction of cost function and wire length. The proposed algorithm was executed with the help of MATLAB and applied it for n100, n200 and n300 to GSRC benchmarks and achieved better run times and reduced overlap occurrence as well as wire length.

In 2015, D Gracia Nirmala Rani et al. [9] presented a novel differential evolution based optimization algorithm for non-slicable floor planning in VLSI. The floorplan structure is constructed using B\*tree representation by taking feasible alignment constraint into consideration. The experiment results are placed as a table of comparison of algorithms SA, ESA, HAS, HGA and DE by taking area as parameter. All the algorithms are implemented on MCNC benchmark circuits and has generated promising results in placement.

In 2014, Shanavas et al. [10] proposed an algorithm for finding optimum solution for VLSI physical design Automation. The authors used Hybrid Genetic algorithm for finding solution. In this article the authors compiled entire physical design computations individually. Genetic Algorithm is used for global optimization. Simulated Annealing for local optimization. The results are formulated as tables with comparison of partitioning optimization using GA with Hybrid algorithms and floor planning optimization using GA with Hybrid algorithms. Placement optimization of Simulated Annealing compared with hybrid algorithms. Routing optimization of Simulated Annealing compared with hybrid algorithms.

In 2013, Xi Chen et al. [11] presented a concept regularity constrained floor planning where they have used Half Perimeter Wire Length (HPWL) model for estimation of wire length and area. This paper discusses about Longest Common Subsequence (LCS) packing algorithm that treats pre packed array blocks as a big block. The floor planning algorithms were implemented in c++ and the results were produced on MCNC benchmark circuits.

In 2013, Deen Md Abdullah et al, [12] introduced clonal selection algorithm for VLSI Floor planning Design. The authors considered preliminaries as floor plan representation, normalized polish expression, floor plan cost, cost function, artificial immune system, clonal selection algorithm. The results are tabulated with standard MCNC and GSRC benchmark in circuits.

In 2013, D Gracia Nirmala Rani et al. [13] a study on B\*tree based evolutionary algorithms for optimization in VLSI floor planning. In this paper different optimization algorithms were discussed for floor planning like Fast Simulated Annealing, Simulate annealing embedded in tabu search, evolutionary and simulated annealing, Hybrid genetic algorithm, differential evolutionary algorithm. All these algorithms are compared by implementing on MCNC benchmark circuits.

In 2013, P Sivaranjani et al. [14] presented method of analyzing the performance of Floor planning in VLSI with the help of evolutionary algorithms. The paper discusses about different optimization algorithms like Particle Swarm Optimization, Hybrid Particle Swarm Optimization, Genetic Algorithm to achieve better placement results. The performance of algorithms is carried out on standard MCNC benchmark circuits by implementing the programs in MATLAB.

In 2012, T. Singha et al. [15] presented an approach based on genetic algorithm for solving VLSI non-slicing floor planning problems. B\* Tree structure is used to represent non slicing floor planning. Authors mentioned this approach of new genetic algorithm as Iterative Prototypes Optimization with Evolved Improvement (POEMS) algorithm. In this algorithm, Genetic algorithm is used to perform local search and it mainly focused on optimization of execution time of algorithm.

In 2011, P Hoyingcharoen et al. [16] proposed fault tolerance in sensor placement optimization using genetic algorithm. The paper aims to give minimum detection probability guaranteed. The authors have pointed the scenarios where sensor nodes fail as evaluator for fault tolerance as well as to use smallest number of sensor nodes to attain minimum detection probability even when some sensor nodes fails to function.

In 2011, Yiqiang Sheng et al. [17] proposed relay race algorithm with which the module placement in VLSI with minimum area to be achieved. The paper also presents comparison of Genetic algorithm, simulated annealing algorithm and the proposed relay race algorithm by which the worst cases of multi objective placement is shown. The experiments were conducted on standard MCNC ami49 benchmark circuit in which 50% improved performance in run time is observed.

In 2010 Jianli Chen et al, [18] shown comparative results of Hybrid genetic algorithm, mDA, Genetic algorithm and memetic algorithm for non slicing hard module VLSI floor planning with B\*Tree representation. The results were shown based on MCNC benchmark circuits performance with HGA. In the results, it has shown that the area of circuit is reduced using Hybrid genetic algorithm.

In 2008, Guolong Chen et al. [19] presented a new technique in which integer coding based on module number is adapted. Algorithm used in this paper is Discrete Particle Swarm optimization with mutation and crossover operators of genetic algorithm incorporated into it for giving better optima. The authors have presented comparison of Simulated Annealing with B\*Tree representation, Particle Swarm intelligence and DPSO algorithms. The experiments employed MCNC and GSRC benchmark circuits and the proposed algorithm gave good result in placement by avoiding solution falling into local minima.

### 3. Experimental investigation of above algorithms

In ASIC design process, there is a need to find out performance of the layout. The key objective of Floor planning is to minimize the area of the chip as well as the delay. This can be achieved by proper placing of the logic blocks. Therefore it is important to predict the interconnections and thereby interconnection delay before the completion of actual routing. Normally it is difficult to predict the interconnects without knowing the source and destination blocks. In this brief, at the floor planning stage, we have got minimum solution for a system with 20 logic blocks. The experimentation has been carried out for 20 blocks with 50 iterations using MATLAB technical computing language. After simulation, the results are shown in figures 1-4. The distribution starts by randomly selecting one block as the reference leading to a routing process based on the condition that every block is arrived at. The best solutions for arranging the blocks randomly in the specified area are achieved for different algorithms. Among the discussed algorithms Genetic Algorithm is giving promising results which are tabulated in the table 1.

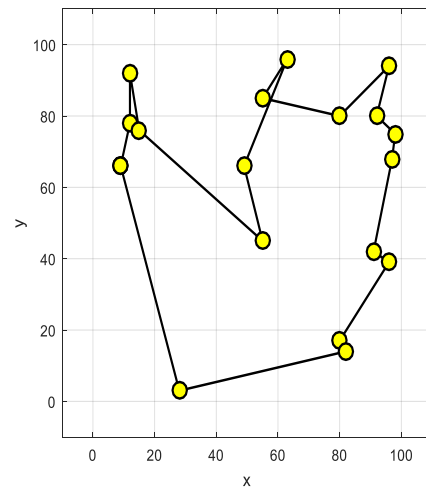


Fig. 5: Simulated Annealing

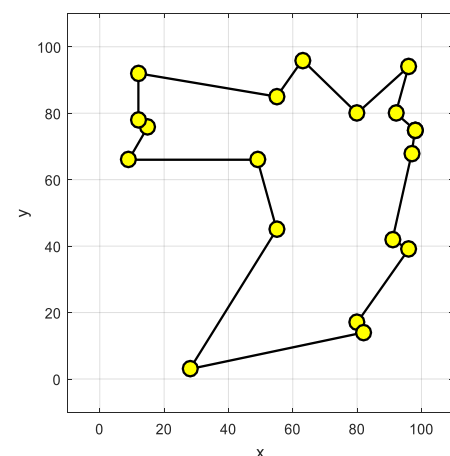


Fig. 6: Tabu Search



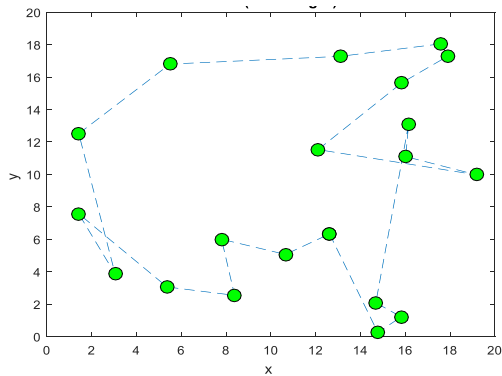


Fig. 7: Ant Colony Algorithm

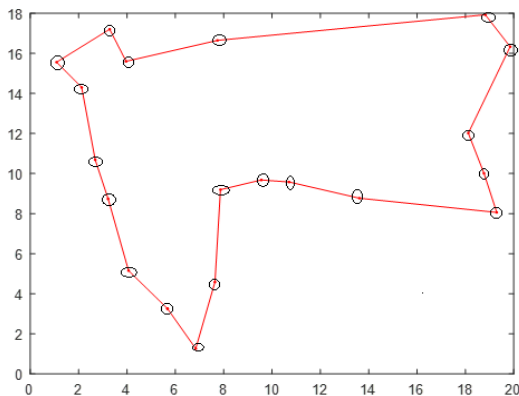


Fig. 8: Genetic Algorithm

Table 1: Comparison of algorithms for 20 blocks

Optimization methods	Simulated Annealing	Tabu search	Ant Colony	Genetic Algorithm
Best Solution	441.05	395.4348	90.90	65.70

The above statistics predicts the location of logic blocks and their minimum wire length.

## 4. Conclusion

In this paper, we have carried out a study on physical design floor planning problem in VLSI. The idea behind this study is to achieve minimum area and wire length while placing the modules in the chip design under floor planning process. The experimental investigation is carried out for 20 blocks with 50 iterations, Genetic algorithm has shown the promising results when compared to the other methods (Simulated annealing, Tabu search, Ant Colony) which were discussed in this paper. Hence these results motivate the researchers to do modifications in the available Genetic algorithm to achieve the results for multiple units.

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