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Research paper

Design and FPGA Implementation of Digital Down Converter for LTE-SDR Receiver

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Abstract

Due to huge demand for high data rate transmission, there is requirement for efficient design of Digital Down Converter (DDC) in wireless communications. DDC is an indispensable part in modern communication, as for higher frequencies it is difficult to down convert the frequency directly to the baseband frequency. Hence a super heterodyne receiver is used to convert the received signal into an intermediate frequency and the intermediate frequency is then converted into the baseband frequency. The architecture of DDC mainly consists of two parts; first one is demodulation and second one is decimation system. The first stage performs the demodulation and the second stage decimation system performs the operation of filtering and decimation. This paper discusses the design and FPGA implementation of DDC for the LTE-SDR receiver for band5 in LTE(UMTS) standards. The design and FPGA implementation of DDC for LTE-SDR is developed and tested using SystemVue software and Xilinx ML507 FPGA board. The results show that simulation results and FPGA implementation results are very close to each other, so the designed DDC can be used in real time LTE SDR application with hardware as FPGA for efficient processing of data with minimum number of resources and at higher operating frequency.

Keywords:*Digital Down Converter; FIR; FPGA; Long Term Evolution(LTE);LPF; NCO;SDR; SystemVue; UMTS; VSA.*

1. Introduction

With the enlargement of mobile environment in day-to-day life the wireless communication has been rapidly increasing in large number of areas. Technology has been improvised for developing universal applications, which has indirectly increased the need for high data rate transmission and also increased the need for high speed multimedia services. This has provoked many groups to study the wireless standard of fourth generation such as Long Term Evolution (LTE) [1] especially used for mobile telecommunication.

LTE works on uplink (from device to tower) and downlink (from tower to device) air interfaces. In downlink, base station is the transmitting part and device is the receiving part, hence we consider the digital signal processing of downlink signals [2]. The LTE signal for downlink uses Orthogonal Frequency Division Multiple Access (OFDMA). In OFDMA multiple sub-carriers are orthogonal to each other to avoid interference with each other. The spectrums of sub-carriers may overlap with each other in frequency domain but the orthogonality means that at a sampling instant, for one sub-carrier all the other sub-carriers are zero valued. This allows the possibility to use the large set of subcarriers without the need of having guard bands between them.

The architecture of Digital Down Converter (DDC) enables the digital IF processing in Software Defined Radio (SDR). The function of DDC [3] is to frequency translate the IF band signal to base band signal centered at 0 Hz.

2. Design of DDC

This paper discusses about the design and FPGA implementation of Digital Down Converter for LTE-SDR receiver. To test the DDC, communication system was desined to give input to DDC. The communication system consists of transmitter, communication channel and receiver.

In digital signal processing, the conversion of digitized, band limited signal to lower frequency at lower sampling rates is called as Digital Down Conversion[4]. The raw radio frequency or intermediate frequency is down converted to complex baseband signal. DDC consists of Numerically Controlled Oscillator (NCO) which generates the sine and cosine signals which are mixed with the In-phase and Quadrature-phase of the signal respectively. This signal is passed through the Low Pass Filter (LPF) which allows difference component which is the baseband frequency and then it is decimated by using decimator which is equivalent to the original signal that is transmitted. The block diagram of the DDC is shown in Fig. 1.

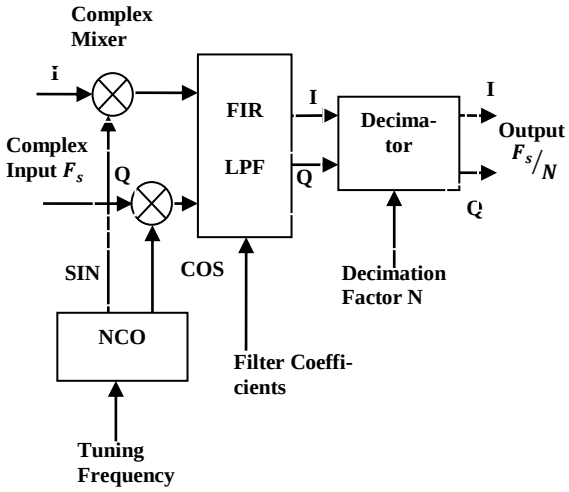

Fig. 1: Block Diagram of DDC.

3. The implementation flow

This paper concentrates on the design of DDC using multiple software such as SystemVue, Xilinx and VSA software. The design process is described in the following steps

1) First the system is designed in SystemVue software and then simulation is done and simulated results are observed
2) Secondly, make sure that whole system is designed in fixed point so that code can be generated from the design
3) Thirdly, generate the VHDL code from the design
4) Fourthly, compile and simulate the generated VHDL code and generate bit file
5) Fifthly, dump the bit file on to ML507 FPGA board and observe the results using Chip Scope Pro Analyzer
6) Finally export the generated Chip Scope data to the SystemVue software to compare the results generated from software and hardware

3.1. Transmitter

The transmitter consists of three sections they are Baseband section, IF section and RF section. In the Baseband section, the baseband signal is generated. The binary signal is generated from the Pseudo-Noise generator in fixed point, the block diagram is shown below Fig.2.

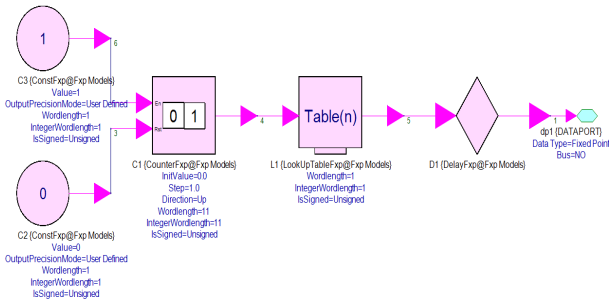

Fig. 2: Schematic Representation of PN Generator.

The Pseudo-Noise generator consists of two fixed point constants one for generating bit one and other for generating bit zero. These are connected to fixed point counter which counts in up direction and is connected to the LUT. The LUT reads the input samples and uses it as an address and writes the samples stored at that address to the output. The generated input signal is shown in Fig.3

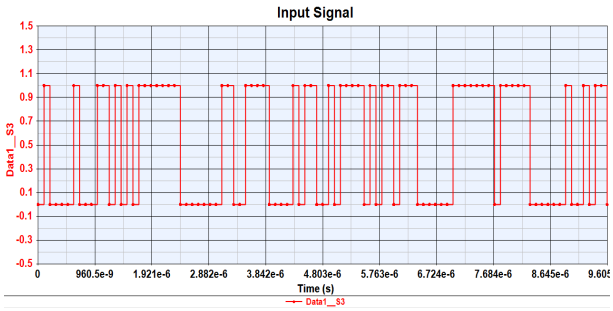

Fig. 3: Input Signal.

The output of the PN generator is a serial data so to convert the data into parallel we are using serial to parallel converter with block size as two. This is connected to fixed point mapper. The mapper groups the consecutive bits to form a symbol value and is then mapped to a complex valued constellation point shown in Fig.4.

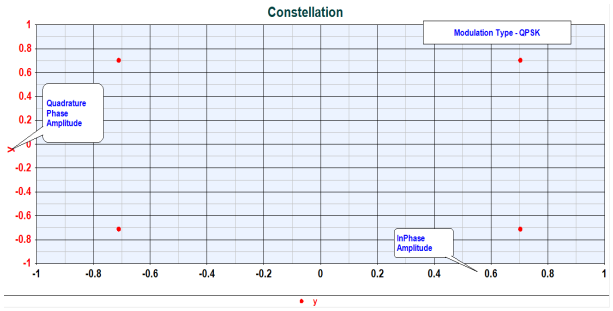

Fig. 4: Constellation Plot.

The constellation point consists of pair of real values (I,Q) which is expressed on the output as I+jQ. I modulates the In-phase component of the carrier and Q modulates the quadrature phase component of the carrier over a symbol period. The symbol length is the number of input bits per symbol. Modulation type selected is QPSK.

The LTE baseband spectrum of bandwidth 5 MHz is generated from the mapper, shown in Fig.5.

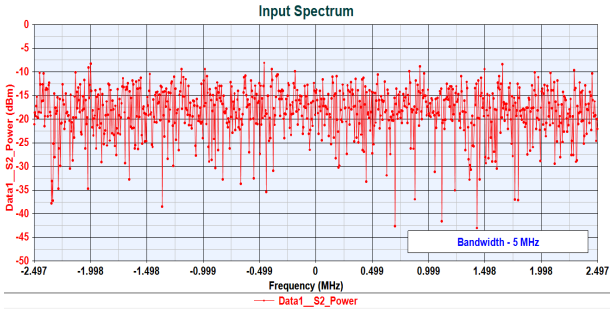

Fig. 5: Input Spectrum.

Now this is converted into IF section that is the baseband frequency is converted into Intermediate Frequency. It is done by up sampling the baseband signal and then passing it through filter and then mixing this signal with the sine and cosine parts generated by the Numerically Controlled Oscillator (NCO), the block diagram is shown in Fig.6.

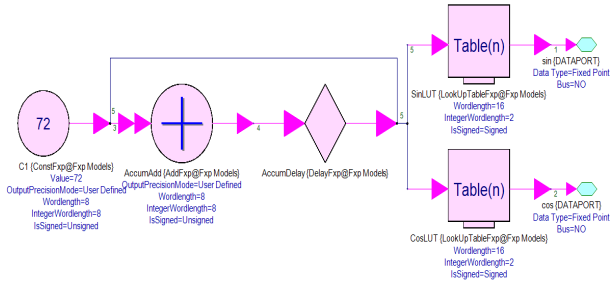

Fig. 6: Schematic Representation of NCO.

The NCO consists of fixed point constant of value 72 and a sampling rate of 50MHz. The NCO generates sine and cosine outputs with a center frequency of 14.0625MHz from the LUTs respectively. This will generate the NCO output spectrum which is shown in Fig.7.

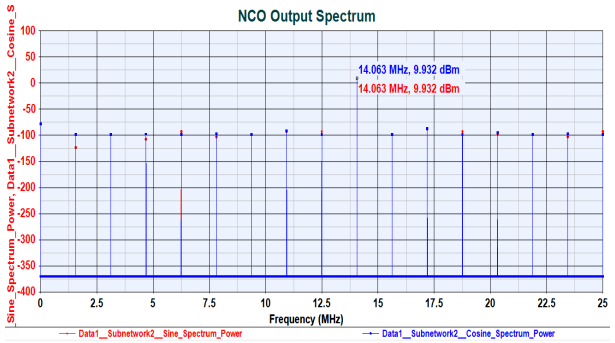

Fig. 7:NCO Output Spectrum.

IF frequency = NCO output - Baseband frequency
IF frequency = 14.0625MHz - 0MHz
IF frequency = 14.0625MHz

The LTE baseband signal is up sampled by a factor of 10 and is passed through a low pass filter having the sampling rate of 50 MHz (5MHz×10). This signal is mixed with sine and cosine parts of the NCO to up convert the signal to IF of 14.0625MHz.

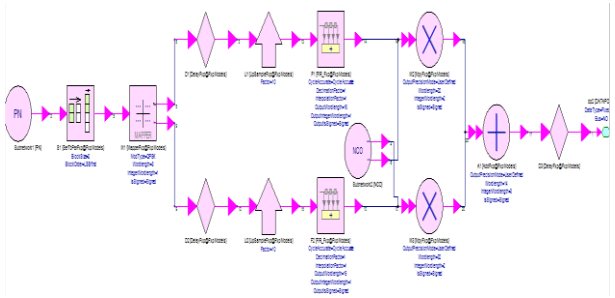

Fig. 8: Schematic Representation of IF Section.

The output of IF section is shown in below Fig. 9. The Fig. 9 is zoomed to view the bandwidth. The sampling frequency is 50MHz.

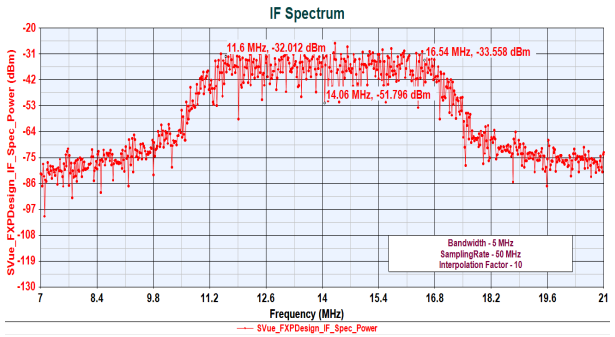

Fig. 9:IF Output Spectrum.

The output of the IF section can be viewed in the Vector Signal Analyzer software with the help of VSA sink. The output of VSA sink at the IF section is shown below. Value of EVM = 0.7%rms which is very low which ensures that the performance of the digital radio is good.

Fig. 10:VSA Output at IF Section.

The IF is again up converted to Radio Frequency for transmission purpose. The IF signal is up sampled by a factor of 64 and passed through a low pass filter of sampling rate 3200MHz (50MHz×64). This signal is now mixed with sine and cosine of another NCO1 to generate RF signal.

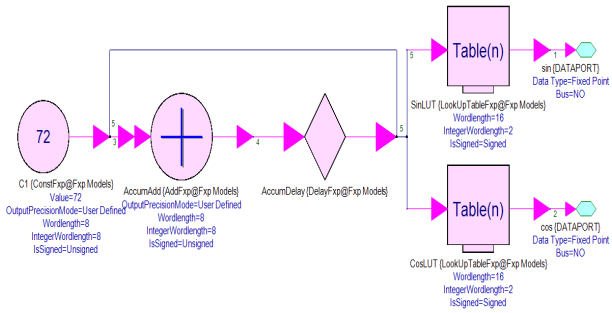

Fig. 11: Schematic Representation of NCO1.

The NCO1 is designed to generate a sine and cosine wave of center frequency 900MHz with a sampling frequency of 3200MHz. The output of the LUTs for sine and cosine signals are shown in Fig. 12.

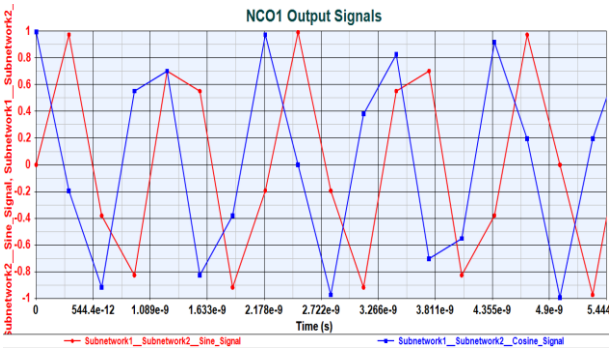

Fig. 12: Sine and Cosine Output Signals of NCO1.

The spectrum output of the sine and cosine LUTs are shown in Fig. 13.

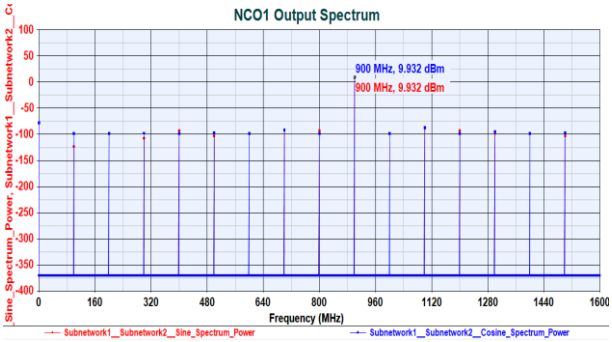

Fig. 13:NCO1 Output Spectrum.

The design of this NCO1 is important because we are developing design for LTE band 5, this center frequency should match with the RF generated from our design. The block diagram of RF section is shown below.

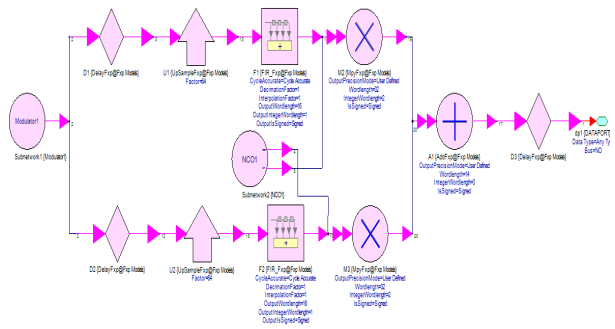

Fig. 14: Schematic Representation of RF Section.

The output of RF section is shown in Fig.15. The RF is centered at 885.93MHz with a sampling rate of 3200MHz.
RF frequency = NCO output - IF frequency
RF frequency = 900MHz - 14.0625MHz
RF frequency = 885.9375MHz.

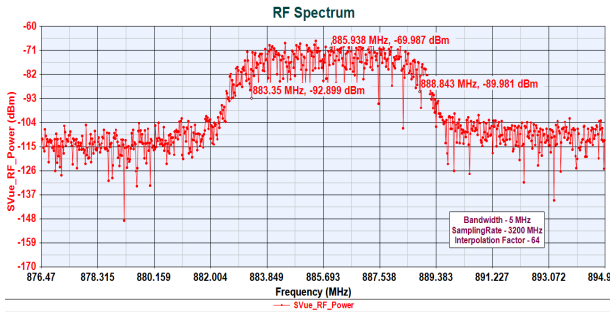

Fig. 15:RF Output Spectrum.

The output of the RF section can be viewed in the Vector Signal Analyzer software with the help of VSA sink. The output of VSA sink at the RF section is shown below.

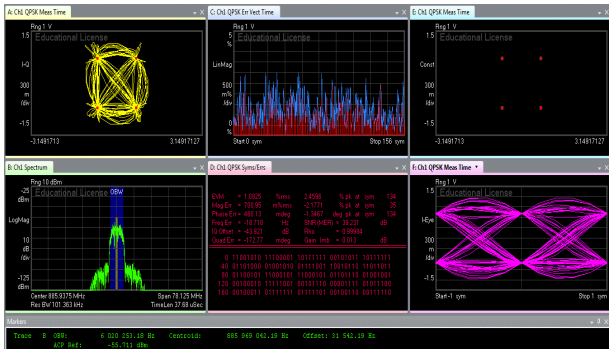

Fig. 16:VSA Output at RF Section.

3.2. Receiver

In the receiver also there are three sections, the input of the receiver is RF signal so there will be a RF section which is the output of the transmitter. The receiver used is superheterodyne receiver. RF signal with center frequency 885.93MHz with 5MHz bandwidth and sampling rate 3200MHz. It is the LTE band5 downlink center frequency. Now this has to be downconverted to the intermediate frequency in the IF section.

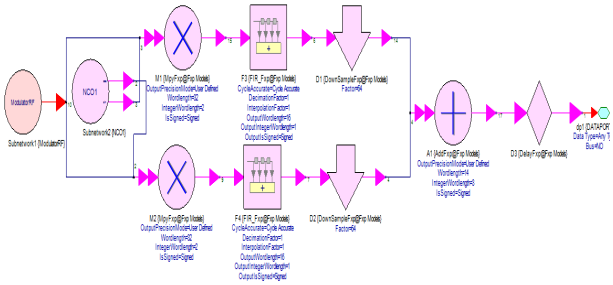

Fig. 17: Schematic Representation of Downconverted IF Section.

In the IF section first demodulation is done and then decimation is done. Demodulation is done by mixing the RF signal with Numerically Controlled Oscillator (NCO1). The output of the RF section in the transmitter is given as input to the mixers and the other input to the mixers are the sine and cosine parts generated from the NCO1 which is same as the one in the transmitter. Drag and drop the NCO1 model in to the schematic.
IF frequency = NCO output - RF frequency
IF frequency = 900MHz - 885.936MHz
IF frequency = 14.0625MHz
The output of the mixers is the downconverted IF spectrum with center frequency 14.0625MHz, bandwidth of 5MHz and sampling rate of 50MHz.

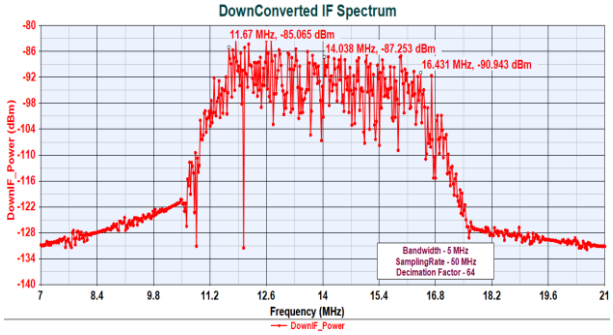

Fig. 18: Downconverted IF Spectrum.

The output of the downconverted IF section is given as input to the baseband section to downconvert the signal from Intermediate Frequency to the Baseband Frequency. First demodulation is done and then decimation is done. In the decimation part first filtering is done and then decimation is done using downsampler to avoid aliasing effect.

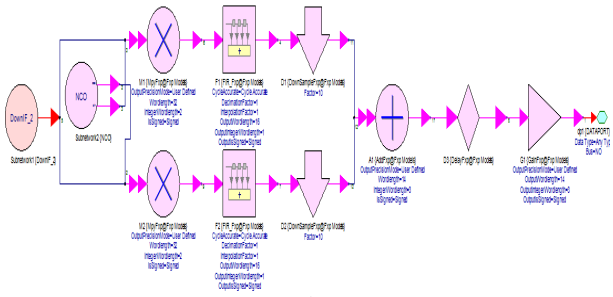

Fig. 19: Schematic Representation of Downconverted Baseband Section.

In the demodulation the output of the CIC filter is given as input to the mixer and the other input to the mixer is Numerically Controlled Oscillator (NCO). The model used here is same as the one which is used in the transmitter. Drag and place the NCO model in to the schematic to give the input to the mixer as shown in the above Fig. 6.
Baseband frequency = NCO output - IF frequency
Baseband frequency = 14.0625MHz - 14.0625MHz
Baseband frequency = 0MHz
The output of the mixers is the down converted spectrum which is the baseband frequency centered at 0MHz with a bandwidth of

5MHz and a sampling rate of 5MHz. The zoom view of the downconverted spectrum is shown below.

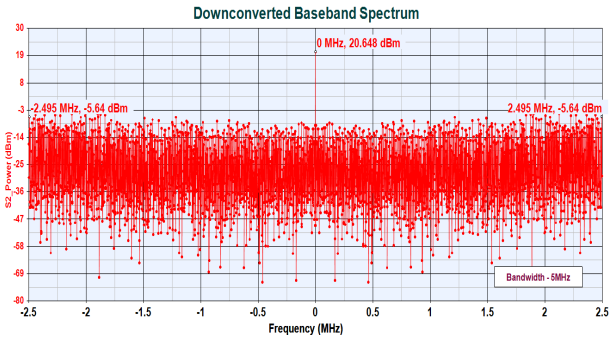

Fig. 20: Downconverted Baseband Spectrum.

Finally it is connected to the fixed point bit extractor to extract the input bits. It extracts a group of bits from the binary word at the input of the token. The bits to be extracted are selected by the MSB and LSB parameters. The output of the bit extractor is shown in Fig.21.

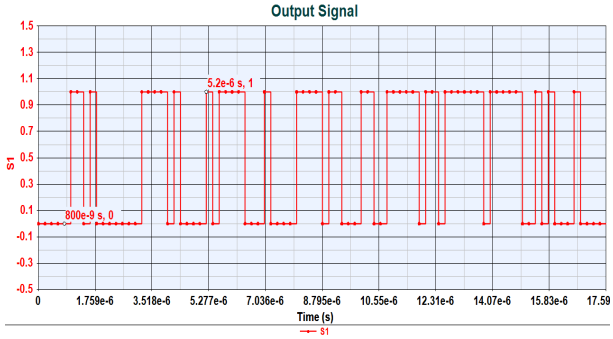

Fig. 21: Output Signal.

4. Implementation on FPGA

The system designed in the SystemVue software is implemented on FPGA board. Xilinx's xc5vfx70t-ff1136 chip is selected to implement the system using VHDL language. In order to implement it in hardware, ILA unit is added to the ChipScope Core Inserter and values has to be assigned to the parameters and connections to the net are specified.

Then bit file is generated to implement it onto FPGA board. FPGA board is connected to PC using JTAG. Configuration of device is done by downloading the bit file on to the FPGA. Output of ChipScope Pro Analyzer is shown below.

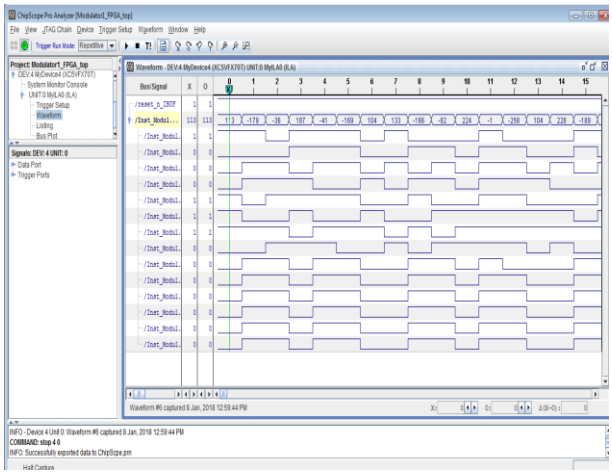

Fig. 22: Output of ChipScope Pro Analyzer.

The device utilization summary of above designed system is shown in Tab 1.

Table 1: Device Utilization Summary

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	7,748	44,800	17%
Number of Slice LUTs	8,517	44,800	19%
Number of fully used LUT-FF pairs	7,246	9,019	80%
Number of bonded IOBs	17	640	2%
Number of Block RAM/FIFO	1	148	0%
Number of BUFG/BUFGCTRLs	3	32	9%
Number of DSP48Es	72	128	56%

The timing summary of above designed system with speed grade -1 is shown in Tab 2.

Table 2: Timing Summary

Timing Summary	
Minimum period	9.014ns
Maximum frequency	110.936MHz
Minimum input arrival time before clock	4.004ns
Maximum output required time after clock	3.264ns

Now, this output of Chip Scope is exported in order to compare the software and hardware results of the designed system. The exported data is been read by the Read File of the SystemVue software.

The block diagram of IF section with FPGA implemented data as input is shown in below Fig. 23.

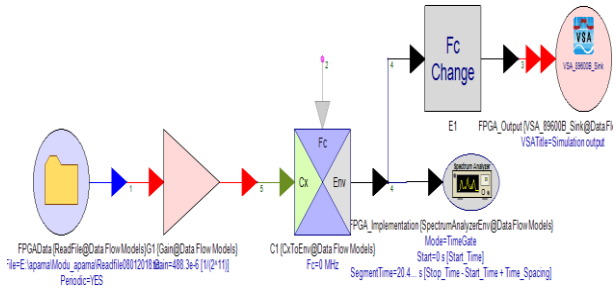

Fig. 23: Schematic Representation of IF Section with FPGA Output Data as Input.

The comparison of output of SystemVue IF section and FPGA implemented IF section is shown in below Fig. 24.

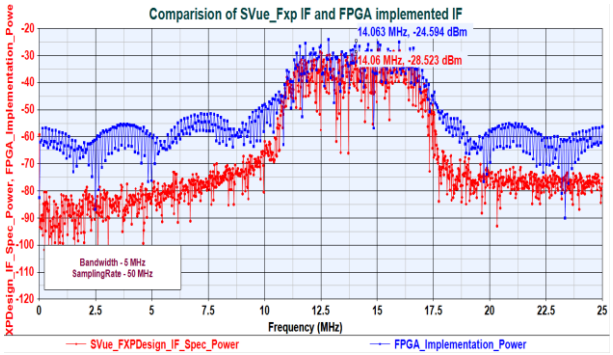

Fig. 24: Comparison of Systemvueand FPGA Implemented IF Section.

The Constellation plot, I-Q diagram, Eye diagram can also be observed using the VSA. The output of the VSA is shown in the below Fig. 25. Value of EVM = 0.7%rms which is very low which ensures that the performance of the digital radio is good at the receiver also.

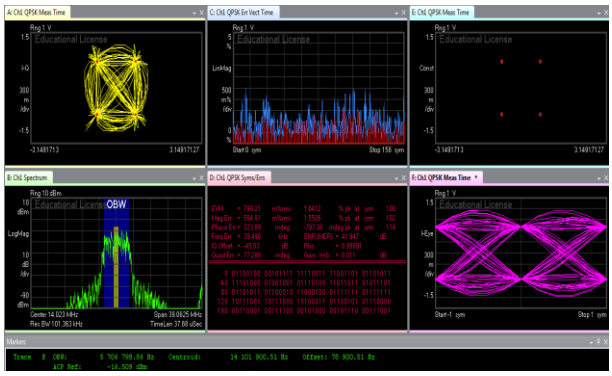

Fig. 25:VSA Output for FPGA Implemented IF Section.

5. Conclusion

An efficient architecture of DDC for wireless communications application for LTE SDR was designed using fixed point filters with frequency band of LTE band5 with center frequency 885.936MHz. The design was done in SystemVue software and implemented on Xilinx ML507 board with devices xc5vfx70t-ff1136 FPGA. The results shows that the designed DDC is producing as per the design specifications and meeting the requirements of baseband processing and comparable to simulation results in SystemVue. It is observed that the proposed DDC design utilizes the minimum resource utilization in terms of DSP48Es and LUTs, and can be operated at a maximum frequency of 110.936MHz.

Acknowledgement

We would like to acknowledge the VFSTR management and Keysight Technologies who provided the Centre of Excellence lab (Keysight Vignan CoE, Advanced RF Microwave and Wireless Communications), where we have used design tool, SystemVue, VSA software. The technical support we received from the engineers from Keysight Technologies is highly appreciated.

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