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Research paper

A 2.4 GHz low noise amplifier design at 130nm CMOS technology using common gate topology for WiFi / WiMAX application

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Abstract

The proposed work shows an innovative designing in TSMC 130nm CMOS technology. A 2.4 GHz common gate topology low noise amplifier (LNA) using an active inductor to attain the low power consumption and to get the small chip size in layout design. By using this Common gate topology achieves the noise figure of 4dB, Forward gain (S_{21}) parameter of 14.7dB, and the small chip size of 0.26 mm, while 0.8mW power consuming from a 1.1V in 130nm CMOS gives the better noise figure and improved the overall performance.

Keywords: *CG LNA, CMOS, TSMC.*

1. Introduction

Over the past decade, many CMOS LNA'S, 802, 11 / 6,802.11 / A and GSM standard has been reported at him from the standards specified by the WiMAX IEEE 802.16e wireless wideband technology. Developed for the existing internet network facilities are inadequate, so that the greatest number of developers is trying to improve this problem.

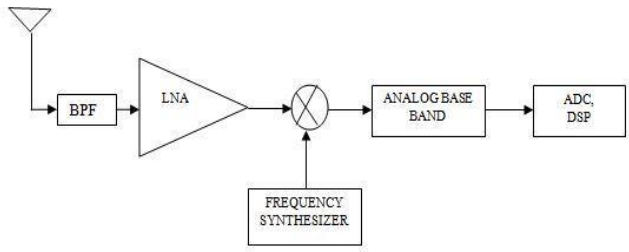

Fig. 1: RF Front end circuit diagram

The CMOS technology is the best solution for low cost, for high integration processing and analog circuits to be mixed with digital. [1].From fig (1), the low noise amplifier is very important block in a receiver section of any communication systems. The gain and noise figure mainly determined performance of the LNA .The LNA is first stage of receiver so that it provides improved input impedance matching.

From the metropolitan area network access systems to cope NLOS (line of sight) and LOS (line of sight) transmission conditions, WiMAX can provide coverage of 75mbps data Rate, Range 50 km. It can extent even 3G Modem, cable, wired by hand wide approach.

Basic LNA requirements:

1. The gain is greater than 10dB to amplify the received signal and to reduce the input referred noise of the subsequent stages.
2. Good linearity: Handling large undesired signals without much distortion.
3. Low noise for high sensitivity
4. The maximum power amplification is 50 ohms for proper operation and can direct the LNA to an antenna that is at an unknown distance regardless of the length of the transmission line.[14]

1.1. Basic topologies

LNA topologies are (a) Resistive termination (b) common gate (c) resistive shunt feedback (d) Inductive degenerated for both narrow and wideband LNA topologies. For better performance parameters like less power, low noise, high gain, low voltage and to optimize low noise amplifier the suitable topology should be choose .The common gate topology, the gain less than 10dB with very low power consumption .Where as the shunt series feedback topology is difficult to parameters among gain, less noise figure and good impedance matching at an input, output with low power consumption and include the noise from the resistor. In inductive degeneration common source the source and gate inductor make the input impedance 50Ω not adding noise from the input. The inductor is off chip at low isolation and the cascade inductor source degeneration is provided isolation of input and output is good, higher gains, lower noise figure and inductor is off chip at low frequency. [1]

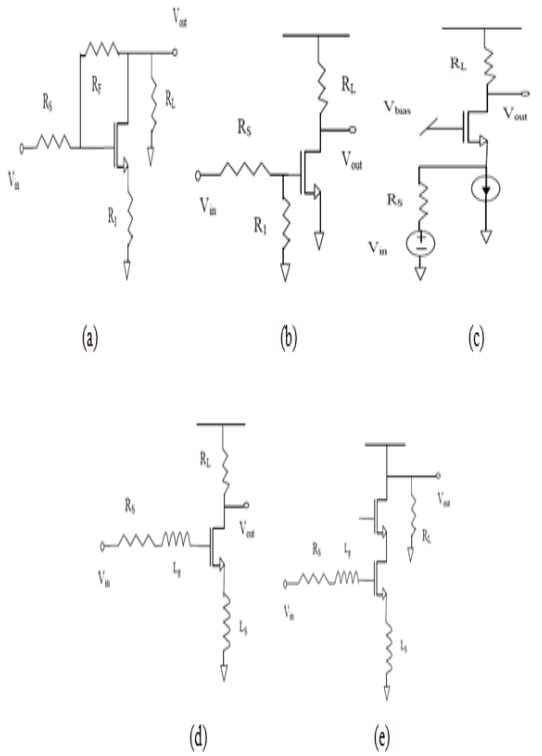

Fig2: Fundamental LNA Topologies:(a) The Shunt Series Feedback Common Source (b) An Inductive Degeneration Common Source (c) Common Gate (d) The Resistive Termination Common Source (e) A Cascode Inductor Source Degeneration[2]

2. Literature survey

After revised different existing proposed LNA topologies and the comparisons of low noise amplifier design criteria have been made to choose the 180nm appropriate schematic circuit for this proposal in 130nm technology. From the comparison in Table 1, the first LNA design is chosen in [3] and has been the excellent performance in term of the parameters gain (db), frequency (GHz), noise figure (db), power supply, power consumption and area/ die size and also that have been compared which is suitable for 130nm technology. Table 1 shows that comparison of the LNA design above**.**

Table.1: Comparistion of performance

	Tec (CMOS) nm	Gain (dB)	Frequency (GHz)	Noise Figure (dB)	Power supply	Power consumption	Area/ die
[3]	180	20	2-3	3.1	1.8	0.5	0.003
[4]	180	19.5	5.2	2.7	3		
[5]	180	15.04	8.72	3.85	1.8	4.7	
[6]	180	17	5.8	3.1	1.8	6.4	
[7]	180	15.7	5.9	1.85	1	19.3	
[8]	180	1.2	3.5	6.5	1.5	10.12	
[9]	180	14.3	2.4	1.6	1.8	0.9	
[10]	180	67.6					
[11]	180	12-14			5.5-6		

3. Design methodology

The Low noise amplifier has mainly divided as three sections as shown in figure.3 below

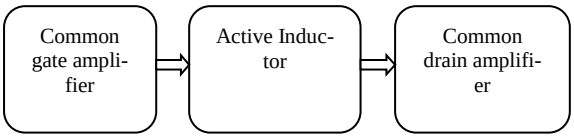

Fig.3: Block diagram of LNA (3)

The each stage as explained in detailed

3.1. Common gate amplifier

This is in all electronic applications because of it is used

a) as current buffer or voltage amplifier circuit .
b) ii. as input stage for LNA amplifier.
c) iii. To obtain an input impedance matching. The input impedance depends on transconductance of CMOS shown in equation

$$Z_{in} = \frac{1}{g_m} \quad (1)$$

d) And it is potentially has low noise performance.

3.2. An active inductor

An active inductor performed the same function as passive inductors and it is a combination of CMOS transistors. The low noise amplifier provides an input and output matching perfectly but in order to design it has difficulty. The layout is easy because of it do not have the magnetic field in the circuit. So that for this proposed design the real active inductor with transistor that performs the same function with active inductor with transistor. Therefore the active inductor has the following advantages for [14]

I lower power consumption.
ii. It is used to minimize chip area in the die.
iii. Used to minimum complexity and easy to implementation.
iv. Used to low cost by minimization of components.
v. At high frequencies to compensate the effect of parasitic capacitors.

Figure 4 and 5 shows the active inductor and its equivalent transistor circuit [8].

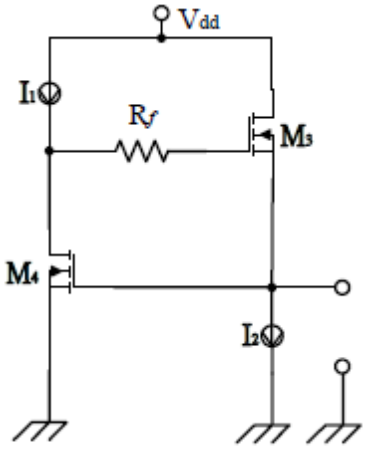

Fig 4: Active Inductor Circuit [3]

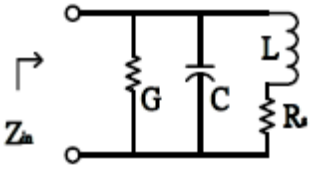

Fig 5: An Active Inductor Circuit [3]

The quality factor (Q), inductance (L) and angular frequency (w) are calculated as follows as shown in figures 4 and 5.

$$L = \frac{C_{gs3}(1+R_f g_{ds4})}{g_{m3} g_{m4}} \quad (2)$$

$$Q = \sqrt{\frac{g_{m3} g_{m4} C_{g3}(1+R_f g_{ds4})}{g^2_{ds4} C_{g4}}} \quad (3)$$

$$\omega = \frac{g_{m3} g_{m4}}{C_{gs3} C_{gs4}(1+R_f g_{ds4})} \quad (4)$$

With double feedback second order of the active inductor is designed with the equivalent circuit shown in Figure 6 for better performance.

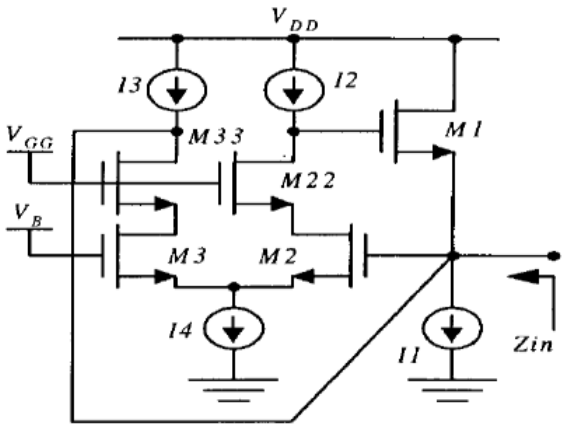

Fig.6: The Double Feedback Second Order Circuit [6]

3.3. The Common Drain Amplifier Description

The Common drain amplifier used as a voltage buffer. The advantages.

1. Used at last stage of LNA.
2. It provides small output impedance at output stage.
3. It has low noise with respect to potentially.[2]

4. The proposed LNA

To achieve the requirements the proposed low noise amplifier circuit uses the active inductor by using the inductor less with 130nm CMOS technology. [3] Based on the improved performance in terms of the parameters like noise figure (N.F), high gain (S_{21}) and lower power consumption the proposed low noise amplifier circuit have been chosen from the above comparison table.

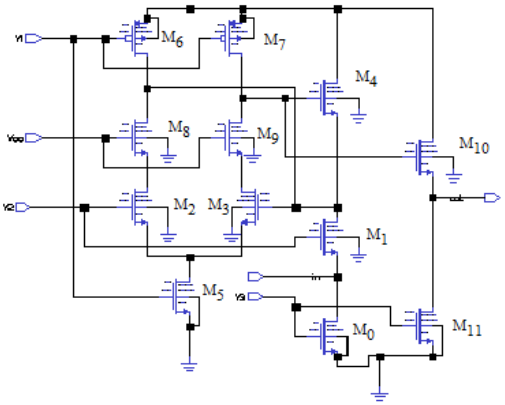

Fig7: Schematic of the LNA to be Improved [2][3]

Table 2: Transistor Width [4]

Transistor	Width
M_O	8µm
M_1, M_2, M_3	12 µm
M_4, M_5	1.8 µm
M_6, M_7	2 µm
M_8 ,M_9	4 µm
M_{10}	3.6 µm
M_{11}	2.7 µm

Table 3: Specifications of LNA design [6]

Parameter	Specification
Supply voltage	1.1V
Gain	>10dB
Noise Figure	< 3dB
Power Consumption	< 50mW
DC Current	< 20mA

An improved low noise amplifier, the DC biasing voltage values for V_1= 1.1v, V_2=0.6v, V_3=0.6v and V_{gg}=0.7v.
In this design, the symbols (W / W) of the transistor, the circuit that is modified. Transistors as long as the reason for being all of it for a different reason to from the width of 0.13µm with the help of the manual calculation. Figure 8 schematic diagram of the proposed LNA plan of Table 4 shows the improvement shown due to gallium. [6]

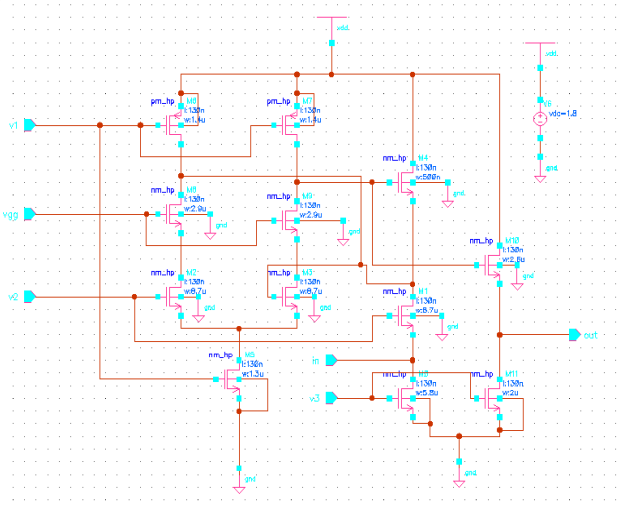

Fig.8: Schematic diagram of the proposed Low Noise Amplifier

Table 4: The Size of new Transistor width at 130nm length

Transistor	Width
M_0	**5.8 µm**
M_1 M_2 M_3	**8.7 µm**
M_4	**0.5 µm**
M_5	**1.3 µm**
M_6 M_7	**1.4 µm**
M_8 M_9	**2.92 µm**
M_{10}	**2.62 µm**
M_{11}	**2.2 µm**

4.1. The Proposed LNA Layout Design

The Layout out of the low noise amplifier is designed by using TSMC 130nm technology with Cadence software tools. It occupies the chip area with small size of 0.26 mm $^{2.}$

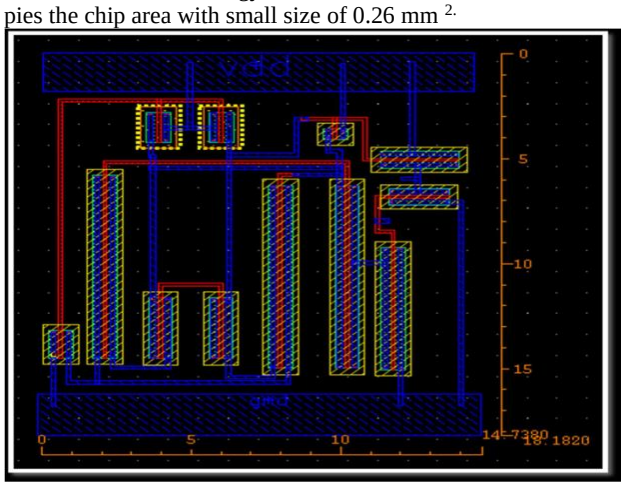

Fig.9: Layout of CGLNA

5. Results and discussion

In the proposed design, the ratio (W / L) of the transistors used was changed. For transistor lengths, the ratio is 130nm for all transistors, whereas the width of the transistor ratio is different, using manual calculation. Figure 8 shows a schematic diagram of the proposed LNA, and Table 4 shows the ratio of transistors after the improvement.

In the design there are serious problems that cause the high value of the win. In the first experiment, all transistors are combined into a single node on the ground. The result shows that the gain value is negative. Thus, it does not meet the requirement of amplification that it should be in positive value. Then it goes on to the second experiment. The grounding nodes are connected to each transistor, respectively. The input value of DC bias for each transistor is different. Therefore, it can be concluded that the ground nodes cannot be combined. Figures 10 and 11 show the gain in the negative value and in the positive value.

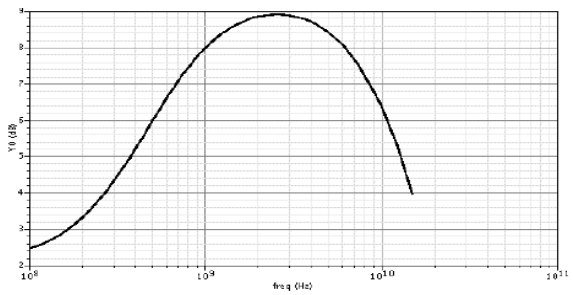

Fig .10: Gain in negative value

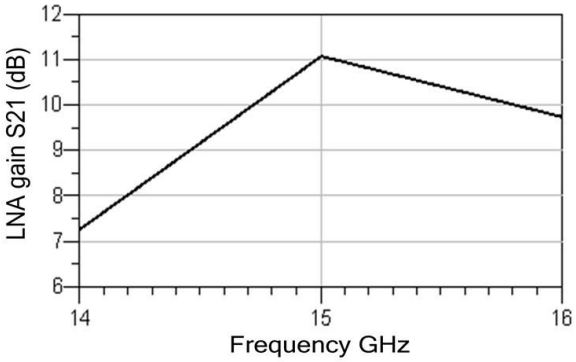

Fig .11: Gain in positive value

After adjusting the DC offset value, Vgg is reduced to 0.5 V, and V1 is increased to 1.2, and the remainder remains the highest gain, which is reached with 14.7 dB. The width of the transistor for M4 also varies by 0.5µm and the noise factor is 4 dB.

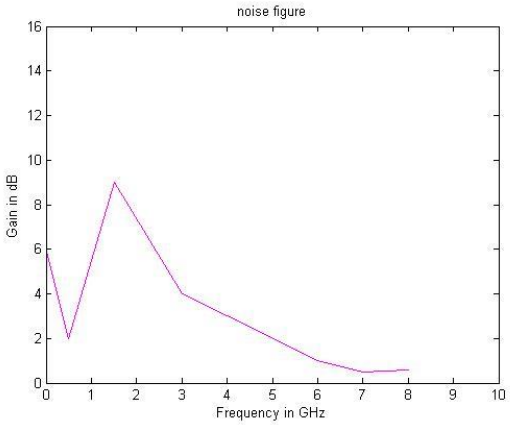

Fig.12: Noise figure (N.F)

5.1.Transient analysis: The circuit will be decided as an amplifier if the output of the circuit is strengthen with applied input signal, that will be done by the transient analysis. The transient analysis of the proposed circuit is shown in fig.13.

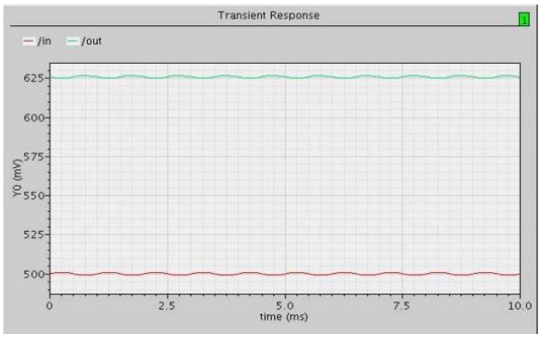

Fig.13: Simulation of Transient response

5.2. AC Analysis result: The amplifier gain is achieved by the AC analysis, mathematically that is using expression

$$Gain = 20\log_{10}\frac{V_{out}}{V_{in}} \quad (5)$$

The gain successfully achieved by this design is 14.7db based on specifications .The simulation result of the parameter forward gain $S_{21}$is 14.7dB shown in figure .14.

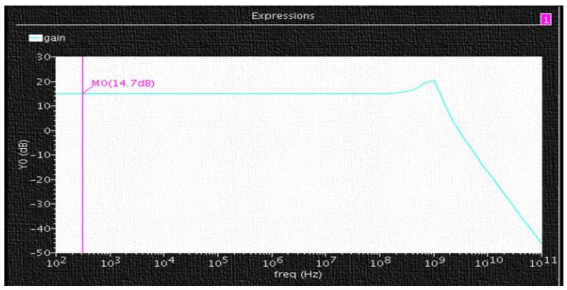

Fig.14: Simulation of AC analysis

6. Conclusion

The proposed improved LNA design at 130 nm was achieved by a gain of 14.7 dB, a noise factor of 4 dB, a very low consumption of 0.8mW, a better adaptation of inputs and outputs and a small size of 0.26 mm.

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